System Event Log (SEL)

Troubleshooting Guide

Summary and definition of events generated by Intel® server boards based on the 1st or 2nd Gen Intel® Xeon® Scalable processor families.

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1. Introduction

The server management hardware that is part of the Intel® Server Boards and Intel® Server Platforms serves as a vital part of the overall server management strategy. The server management hardware provides essential information to the system administrator and provides the administrator the ability to remotely control the server, even when the operating system is not running.

The Intel Server Boards and Intel Server Platforms offer comprehensive hardware and software based solutions. The server management features make the servers simple to manage and provide alerting on system events. From entry to enterprise systems, good overall server management is essential to reduce overall total cost of ownership.

This troubleshooting guide is intended to help the users better understand the events that are logged in the Baseboard Management Controllers (BMC) System Event Logs (SEL) on these Intel Server Boards.

There is a separate user guide that covers the general server management and the server management software offered on the Intel Server Boards and Intel Server Platforms.

This document supports the following Intel Server products currently supported by this document:

- Intel® Server Board based on Intel® Xeon® processor E5-1600/2600/4600 v2 product family
- Intel® Server Board based on Intel® Xeon® processor E5-2400 v2 product family
- Intel® Server Board based on Intel® Xeon® processor E5-2600 v3/v4 product family
- Intel® Server Board based on Intel® Xeon® processor E3-1200 v2/v3/v4 product family
- Intel® Server Board based on Intel® Xeon® processor E3-1200 v5/v6 product family
- Intel® Server Board based on Intel® Xeon Phi™ product family
- Intel® Server Board based on Intel® Xeon® Scalable processor family
- Intel® Server Board based on 2nd Gen Intel® Xeon® Scalable processor family
- Intel® Server Board based on Intel® Xeon® Platinum 9200 processor family

1.1 Purpose

The purpose of this document is to list all possible events generated by the Intel platform. It may be possible that other sources (not under Intel's control) also generate events, which are not described in this document.

1.2 Industry Standards

1.2.1 Intelligent Platform Management Interface (IPMI)

The key characteristic of the Intelligent Platform Management Interface (IPMI) is that the inventory, monitoring, logging, and recovery control functions are available independently of the main processors, BIOS, and operating system. Platform management functions can also be made available when the system is in a power-down state.

IPMI works by interfacing with the BMC, which extends management capabilities in the server system and operates independently of the main processor by monitoring the onboard instrumentation. Through the BMC, IPMI also allows administrators to control power to the server and remotely access BIOS configuration and operating system console information.

IPMI defines a common platform instrumentation interface to enable interoperability between:

- The baseboard management controller and chassis;
- The baseboard management controller and systems management software; and
- Between servers.

IPMI enables the following:

- Common access to platform management information, consisting of
  - Local access from systems management software;
  - Remote access from LAN;
  - Inter-chassis access from Intelligent Chassis Management Bus; and
  - Access from LAN, serial/modem, IPMB, PCI SMBus*, or ICMB, available even if the processor is down.
- Isolation of systems management software from hardware.
- Ability to make hardware advancements without impacting the systems management software.
- Facilitation of cross-platform management software.

Find more information on IPMI at http://www.intel.com/design/servers/ipmi.

1.2.2 Baseboard Management Controller (BMC)

A baseboard management controller (BMC) is a specialized microcontroller embedded on most Intel Server Boards. The BMC is the heart of the IPMI architecture and provides the intelligence behind intelligent platform management, that is, the autonomous monitoring and recovery features implemented directly in platform management hardware and firmware.

Different types of sensors built into the computer system report to the BMC on parameters such as: temperature, cooling fan speeds, power mode, operating system status, and so on. The BMC monitors the system for critical events by communicating with various sensors on the system board; it sends alerts and logs events when certain parameters exceed their preset thresholds, indicating a potential failure of the system. The administrator can also remotely communicate with the BMC to take some corrective action such as resetting or power cycling the system to get a hung operating system running again. These abilities save on the total cost of ownership of a system.

For Intel server boards and Intel server platforms, the BMC supports the industry standard *IPMI 2.0 Specification*, enabling remote configuration, monitoring, and systems recovery.

1.2.2.1 System Event Log (SEL)

The BMC provides a centralized, non-volatile repository for critical, warning, and informational system events called the System Event Log (SEL). By having the BMC manage the SEL and logging functions, it helps to ensure that “post-mortem” logging information is available if a failure occurs that disables the system processor(s).

The BMC allows access to the SEL from in-band and out-of-band mechanisms. There are various tools and utilities that can be used to access the SEL including the SEL Viewer utility and multiple open sourced IPMI tools.

1.2.3 Intel® Intelligent Power Node Manager Version 3.0

Intel® Intelligent Power Node Manager version 3.0 is a platform-resident technology that enforces power and thermal policies for the platform. These policies are applied by exploiting subsystem knobs (such as processor P and T states) that can be used to control power consumption. Intel Intelligent Power Node Manager enables data center power and thermal management by exposing an external interface to management software through which platform policies can be specified. It also enables specific data center power management usage models such as power limiting.

The configuration and control commands are used by the external management software or BMC to configure and control the Intel Intelligent Power Node Manager feature. Because the platform firmware does not have any external interface, external commands are first received by the BMC over LAN and then relayed to the platform firmware over Intelligent Power Management Bus (IPMB) channel. The BMC acts as a relay

and the transport conversion device for these commands. For simplicity, the commands from the management console might be encapsulated in a generic CONFIG packet format (configuration data length, configuration data blob) to the BMC so that the BMC does not even have to parse the actual configuration data.

The BMC provides the access point for remote commands from external management software and generates alerts to them. Intel Intelligent Power Node Manager on Intel® Management Engine (Intel® ME) is an IPMI satellite controller. A mechanism exists to forward commands to Intel ME and then sends the response back to originator. Similarly events from Intel ME are sent as alerts outside of the BMC.

2. Basic Decoding of a SEL Record

The System Event Log (SEL) record format is defined in the *IPMI Specification*. The following sections provide a basic definition for each of the fields in a SEL. For more details, see the *IPMI Specification*.

The definitions for the standard SEL can be found in Table 1.

The definitions for the OEM defined event logs can be found in Table 3 and Table 4.

2.1 Default Values in the SEL Records

Unless otherwise noted in the event record description, the following are the default values for all SEL entries.

- Byte [3] = Record Type (RT) = `02h` = System event record
- Byte [9:8] = Generator ID = `0020h` = BMC firmware
- Byte [10] = Event Message Revision (ER) = `04h` = IPMI 2.0

Table 1. SEL record format

Byte	Field	Description
1, 2	Record ID (RID)	ID used for SEL record access.
3	Record Type (RT)	[7:0] – Record type `02h` = System event record (default) `C0h-DFh` = OEM timestamped, bytes 8–16 OEM defined (see Table 3) `E0h-FFh` = OEM non-timestamped, bytes 4–16 OEM defined (see Table 4)
4–7	Timestamp (TS)	Time when the event was logged. The least significant byte is first. For example, TS:[29][76][68][4C] = `4C687629h` = 1281914409 = Sun, 15 Aug 2010 23:20:09 UTC **Note**: There are various websites that convert the raw number to a date/time.
8, 9	Generator ID (GID)	RqSA and LUN if event was generated from IPMB. Software ID if event was generated from system software. *Byte 1* [7:1] – 7-bit I^2C secondary address, or 7-bit system software ID [0] – `0b` = ID is IPMB secondary address, `1b` = System software ID Software ID values: `0001h` – BIOS POST for POST errors, RAS configuration/state, timestamp synch, operating system boot events `0033h` – BIOS SMI handler `0020h` – BMC firmware (default) `002Ch` – Intel ME firmware `0041h` – Server management software `00C0h` – HSC firmware – HSBP A `00C2h` – HSC firmware – HSBP B *Byte 2* [7:4] – Channel number. Channel that event message was received over. `0h` if the event message was received from the system interface, primary IPMB, or internally generated by the BMC. [3:2] – Reserved. Write as 00b. [1:0] – IPMB device LUN if byte 1 holds secondary address. `00b` otherwise.
10	EvM Rev (ER)	Event message format version. `04h` = IPMI v2.0 (default) `03h` = IPMI v1.0
11	Sensor Type (ST)	Sensor type code for sensor that generated the event.
12	Sensor # (SN)	Number of the sensor that generated the event (from SDR).

Byte	Field	Description
13	Event Dir/Event Type (EDIR)	*Event Dir* [7] – 0b = Assertion event, 1b = Deassertion event. *Event Type* Type of trigger for the event. For example, critical threshold going high, state asserted, and so on. Also indicates class of the event; for example, discrete, threshold, or OEM. The Event Type field is encoded using the Event/Reading Type Code. [6:0] – Event Type Codes 01h = Threshold (states = 0x00-0x0b) 02h-0ch = Discrete 6Fh = Sensor-specific 70-7Fh = OEM
14	Event Data 1 (ED1)	See Table 2.
15	Event Data 2 (ED2)	
16	Event Data 3 (ED3)	

Table 2. Event request message event data field contents

Sensor Class	Event Data
Threshold	*Event Data 1* [7:6] – 00b = Unspecified Event Data 2 01b = Trigger reading in Event Data 2 10b = OEM code in Event Data 2 11b = Sensor-specific event extension code in Event Data 2 [5:4] – 00b = Unspecified Event Data 3 01b = Trigger threshold value in Event Data 3 10b = OEM code in Event Data 3 11b = Sensor-specific event extension code in Event Data 3 [3:0] – Offset from Event/Reading Code for threshold event. *Event Data 2* – Reading that triggered event, FFh or not present if unspecified. *Event Data 3* – Threshold value that triggered event, FFh or not present if unspecified. If present, Event Data 2 must be present.
Discrete	*Event Data 1* [7:6] – 00b = Unspecified Event Data 2 01b = Previous state and/or severity in Event Data 2 10b = OEM code in Event Data 2 11b = Sensor-specific event extension code in Event Data 2 [5:4] – 00b = Unspecified Event Data 3 01b = Reserved 10b = OEM code in Event Data 3 11b = Sensor-specific event extension code in Event Data 3 [3:0] – Offset from Event/Reading Code for discrete event state *Event Data 2* [7:4] – Optional offset from "Severity" Event/Reading Code (0Fh if unspecified). [3:0] – Optional offset from Event/Reading Type Code for previous discrete event state (0Fh if unspecified). *Event Data 3* – Optional OEM code. FFh or not present if unspecified.

Sensor Class	Event Data
OEM	*Event Data 1* [7:6] – 00b = Unspecified in Event Data 2 01b = Previous state and/or severity in Event Data 2 10b = OEM code in Event Data 2 11b = Reserved [5:4] – 00b = Unspecified Event Data 3 01b = Reserved 10b = OEM code in Event Data 3 11b = Reserved [3:0] – Offset from Event/Reading Type Code *Event Data 2* [7:4] – Optional OEM code bits or offset from "Severity" Event/Reading Type Code (0Fh if unspecified). [3:0] – Optional OEM code or offset from Event/Reading Type Code for previous event state (0Fh if unspecified). *Event Data 3* – Optional OEM code. FFh or not present if unspecified.

Table 3. OEM SEL record (type C0h-DFh)

Byte	Field	Description
1, 2	Record ID (RID)	ID used for SEL Record access.
3	Record Type (RT)	[7:0] – Record Type C0h-DFh = OEM timestamped, bytes 8–16 OEM defined
4–7	Timestamp (TS)	Time when the event was logged. The least significant byte is first. For example, TS:[29][76][68][4C] = 4C687629h = 1281914409 = Sun, 15 Aug 2010 23:20:09 UTC **Note**: There are various websites that convert the raw number to a date/time.
8–10	Manufacturer ID	The least significant byte is first. The manufacturer ID is a 20-bit value that is derived from the IANA "Private Enterprise" ID. Most significant four bits = Reserved (0000b). 000000h = Unspecified, 0FFFFFh = Reserved. This value is binary encoded. For example, the ID for the IPMI forum is 7154 decimal, which is 1BF2h, which will be stored in this record as F2h, 1Bh, and 00h for bytes 8 through 10, respectively.
11–16	OEM Defined	Defined according to the manufacturer identified by the Manufacturer ID field.

Table 4. OEM SEL record (type E0h-FFh)

Byte	Field	Description
1, 2	Record ID (RID)	ID used for SEL Record access.
3	Record Type (RT)	[7:0] – Record Type E0h-FFh = OEM system event record
4–16	OEM	OEM Defined. This is defined by the system integrator.

2.2 Notes on SEL Logs and Collecting SEL Information

When capturing the SEL log, always collect both the text/human readable version and the hex version. Because some of the data is OEM-specific, some utilities cannot decode the information correctly. In addition, with some OEM-specific data there may be additional variables that are not decoded at all.

The following section provides examples of not decoding all the information.

See section 2.2.1 for the PCIe* errors. The type of error and the PCI Bus, Device, and Function are all a part of Event Data 1 through Event Data 3.

See section 2.2.2 for the Power Supply events. When there is a failure, predictive failure, or a configuration error, Event Data 2 and Event Data 3 hold additional information describing the Power Supply PMBus Command Registers and values for that particular event.

2.2.1 Example of Decoding a PCIe* Correctable Error Events

The following is an example of decoding a PCIe correctable error event. For this particular event, it recorded a receiver error on Bus 0, Device 2, and Function 2. Correctable errors are acceptable and normal at a low rate of occurrence.

RID[27][00] RT[02] TS[0A][9B][2E][50] GID[33][00] ER[04] ST[13] SN[05] EDIR[71] ED1[A0] ED1[00] ED3[12]
- RID (Record ID) = 0027h
- RT (Record Type) = 02h = system event record
- TS (Timestamp) = 502E9B0Ah
- GID (Generator ID = 0033h = BIOS SMI Handler
- ER (Event Message Revision) = 04h = IPMI v2.0
- ST (Sensor Type) = 13h = Critical Interrupt (From *IPMI Specification* Table 42-3, Sensor Type Codes)
- SN (Sensor Number = 05h
- EDIR (Event Direction/Event Type) = 71h
  - [7] = 0b = Assertion Event
  - [6:0] = 71h = OEM Specific for PCI Express* correctable errors
- ED1 (Event Data 1) = A0h
  - [7:6] = 10b = OEM code in Event Data 2
  - [5:4] – 10b = OEM code in Event Data 3
  - [3:0] – Event Trigger Offset = 0h = Receiver Error
- ED2 (Event Data 2) = 00h; PCI Bus number = 0h
- ED3 (Event Data 3) = 12h
  - [7:3] – PCI Device number = 02h
  - [2:0] – PCI Function number = 2h

2.2.2 Example of Decoding a Power Supply Predictive Failure Event

The following is an example of decoding a Power Supply predictive failure event. For this example, power supply 1 saw an AC power loss event with both the input under-voltage warning and fault events getting set. In most cases, this means that the AC power spiked under the minimum warning and fault thresholds for over 20 milliseconds but the system remained powered on. If these events continue to occur, it is advisable to check the power source.

RID[5D][00] RT[02] TS[D3][B1][AE][4E] GID[20][00] ER[04] ST[08] SN[50] EDIR[6F] ED1[A2] ED2[06] ED3[30]
- RID (Record ID) = 005Dh
- RT (Record Type) = 02h = system event record
- TS (Timestamp) = 4EAEB1D3h
- GID (Generator ID = 0020h = BMC
- ER (Event Message Revision) = 04h = IPMI v2.0
- ST (Sensor Type) = 08h = Power Supply (From *IPMI Specification* Table 42-3, Sensor Type Codes)
- SN (Sensor Number = 50h = Power Supply 1

EDIR (Event Direction/Event Type) = 6Fh
- [7] = 0b = Assertion Event
- [6:0] = 6fh = Sensor specific

ED1 (Event Data 1) = A2h
- [7:6] = 10b = OEM code in Event Data 2
- [5:4] – 10b = OEM code in Event Data 3
- [3:0] – Event Trigger Offset = 2h = Predictive Failure

ED2 (Event Data 2) = 06h = Input under-voltage warning

ED3 (Event Data 3) = 30h; From *PMBus Specification* STATUS_INPUT command
- [5] – VIN_UV_WARNING (Input Under-voltage Warning) = 1b
- [4] – VIN_UV_FAULT (Input Under-voltage Fault) = 1b

2.2.3 Example of Decoding an NVMe* Temperature Sensor Event

The following is an example of decoding an NVMe* temperature sensor event. The NVMe temperature SEL occurs when the aggregate temperature sensor reading reaches the upper critical threshold. To report which of several drives are over temperature, OEM extended data bytes are used. The remainder of the SEL uses standard temperature sensor decoding rules.

The NVMe temperature SEL uses a new format for the OEM extended data bytes. See the *Intel® Server System Integrated Baseboard Management Controller Firmware External Product Specification*.

ExtData[0] already has an established format. Bits 0–1 define the severity of the SEL. Bits 4–6 define the number of extended data bytes. Bits 2–3 and 7 are reserved. The new format is detailed below.

ExtData[0]
- [7] = Extended format indicator
- [6:4] = # Extended Data bytes
- [3:2] = reserved
- [1:0] = Existing severity encoding

ExtData[1] = Extended Format Byte Code
- 0 = Reserved
- 1 = Drive Position Format
- 2 = Critical Warning Format
- 3 = Add-in card format
- 4-0xff = Reserved

ExtData[2]
- For Format = 1 (Drive Position Format), ExtData[2] is a bitfield indicating which drives are over temperature. Bit 0 set indicates Drive 0 is over temp. Bit 7 set indicates Drive 7 is over temp.

Exertion example:

RID:0099 RT:02 TS:558BEF64 GID:0020 ER:04 ST:01 S#:92 ET:01 ED:59 01 00 OEM:A2 01 20 FF FF FF FF FF
- ExtData[0] = 0xA2
  - Bit 7 set, so ExtData[1] is format indicator
  - Bit 6-4 = 2, indicating 2 more OEM bytes (format, bitfield)
  - Bit 1–0 = 2, indicating this is a Critical SEL
- ExtData[1] = 0x01, indicating Drive Position Format
- ExtData[2] = 0x20, indicating drive slot 5 (zero based) is over temp

3. Sensor Cross-References List

This chapter contains cross-references to help find details on any specific SEL entry.

3.1 BMC-Owned Sensors (GID = 0020h)

The following table can be used to find the details of sensors owned by the BMC.

Table 5. BMC-owned sensors

Sensor #	Sensor Name	Details Section	Next Steps
01h	Power Unit Status (Pwr Unit Status)	4.4.1	Table 25
02h	Power Unit Redundancy (Pwr Unit Redund)	4.4.2	Table 27
03h	IPMI Watchdog (IPMI Watchdog)	11.1	Table 98
04h	Physical Security (Physical Scrty)	10.1	Table 94
05h	FP Interrupt (FP NMI Diag Int)	10.2	Section 10.2.1
06h	SMI Timeout (SMI Timeout)	11.2	Section 11.2.1
07h	System Event Log (System Event Log)	11.3	Not applicable
08h	System Event (System Event)	11.4	Section 11.4.1
09h	Button Sensor (Button)	10.3	Not applicable
0Ah	BMC Watchdog (BMC Watchdog)	11.5	Section 11.5.1
0Bh	Voltage Regulator Watchdog (VR Watchdog)	4.3	Section 4.3.1
0Ch	Fan Redundancy (Fan Redundancy)	5.1.2	Table 43
0Dh	SSB Thermal Trip (SSB Thermal Trip)	5.2.5	Section 5.2.5.3
0Eh	IO Module Presence (IO Mod Presence)	11.8	Section 11.8.1
0Fh	SAS Module Presence (SAS Mod Presence)	11.8	Section 11.8.1
10h	BMC Firmware Health (BMC FW Health)	11.6	Section 11.6.1
11h	System Airflow (System Airflow)	5.3	Not applicable
12h	Firmware Update Status (FW Update Status)	11.7	Not applicable
13h	IO Module2 Presence (IO Mod2 Presence)	11.8	Section 11.8.1
14h	Baseboard Temperature 5 (Platform Specific)	5.2.1	Table 46
15h	Baseboard Temperature 6 (Platform Specific)	5.2.1	Table 46
16h	IO Module2 Temperature (I/O Mod2 Temp)	5.2.1	Table 46
17h	PCI Riser 3 Temperature (PCI Riser 3 Temp)	5.2.1	Table 46
18h	PCI Riser 4 Temperature (PCI Riser 4 Temp)	5.2.1	Table 46
1Ah	Firmware Security(FW Security)	11.13	Section 11.13
20h	Baseboard Temperature 1 (Platform Specific)	5.2.1	Table 46
21h	Front Panel Temperature (Front Panel Temp)	5.2.1	Table 46
22h	SSB Temperature (SSB Temp)	5.2.1	Table 46
23h	Baseboard Temperature 2 (Platform Specific)	5.2.1	Table 46
24h	Baseboard Temperature 3 (Platform Specific)	5.2.1	Table 46
25h	Baseboard Temperature 4 (Platform Specific)	5.2.1	Table 46
26h	IO Module Temperature (I/O Mod Temp)	5.2.1	Table 46
27h	PCI Riser 1 Temperature (PCI Riser 1 Temp)	5.2.1	Table 46
28h	IO Riser Temperature (IO Riser Temp)	5.2.1	Table 46
29h–2Bh	Hot-Swap Back Plane 1–3 Temperature (HSBP 1–3 Temp)	12.1	Table 117
2Ch	PCI Riser 2 Temperature (PCI Riser 2 Temp)	5.2.1	Table 46
2Dh	SAS Module Temperature (SAS Mod Temp)	5.2.1	Table 46

Sensor #	Sensor Name	Details Section	Next Steps
2Eh	Exit Air Temperature (Exit Air Temp)	5.2.1	Table 46
2Fh	Network Interface Controller Temperature (LAN NIC Temp)	5.2.1	Table 46
30h-3Fh	Fan Tachometer Sensors (Chassis specific sensor names)	5.1.1	Table 39
40h-4Fh	Fan Present Sensors (Fan x Present)	5.1.2	Table 41
50h	Power Supply 1 Status (PS1 Status)	4.5.1	Table 25
51h	Power Supply 2 Status (PS2 Status)	4.5.1	Table 25
52h	Power Supply 3 Status (PS3 Status)	4.5.1	Table 25
54h	Power Supply 1 AC Power Input (PS1 Power In)	4.5.2	Table 32
55h	Power Supply 2 AC Power Input (PS2 Power In)	4.5.2	Table 32
56h	Power Supply 3 AC Power Input (PS2 Power In)	4.5.2	Table 32
58h	Power Supply 1 +12V % of Maximum Current Output (PS1 Curr Out %)	4.5.3	Table 34
59h	Power Supply 2 +12V % of Maximum Current Output (PS2 Curr Out %)	4.5.3	Table 34
5Ah	Power Supply 3 +12V % of Maximum Current Output (PS3 Curr Out %)	4.5.3	Table 34
5Ch	Power Supply 1 Temperature (PS1 Temperature)	4.5.4	Table 36
5Dh	Power Supply 2 Temperature (PS2 Temperature)	4.5.4	Table 36
5Eh	Power Supply 3 Temperature (PS3 Temperature)	4.5.4	Table 36
60h-68h	Hard Disk Drive 15–23 Status (HDD 15–23 Status)	12.2	Table 119
69h-6Bh	Hot-Swap Controller 1–3 Status (HSC1-3 Status)	12.3	Section 12.3.1
70h	Processor 1 Status (P1 Status)	6.1	Table 60
71h	Processor 2 Status (P2 Status)	6.1	Table 60
72h	Processor 3 Status (P3 Status)	6.1	Table 60
73h	Processor 4 Status (P4 Status)	6.1	Table 60
74h	Processor 1 Thermal Margin (P1 Therm Margin)	5.2.2	Table 49
75h	Processor 2 Thermal Margin (P2 Therm Margin)	5.2.2	Table 49
76h	Processor 3 Thermal Margin (P3 Therm Margin)	5.2.2	Table 49
77h	Processor 4 Thermal Margin (P4 Therm Margin)	5.2.2	Table 49
78h-7Bh	Processor 1–4 Thermal Control % (P1-P4 Therm Ctrl %)	5.2.3	Section 5.2.3.1
7Ch	Processor ERR2 Timeout (CPU ERR2)	6.6	Section 6.6.1
7Dh	IERR recovery dump info (IERR Rec Info)	6.3	Section 6.3.1
80h	Internal Error (IERR)	6.2	Table 62
82h	Processor Population Fault (CPU Missing)	6.3	Section 6.3.1
83h-86h	Processor 1–4 DTS Thermal Margin (P1-P4 DTS Therm Mgn)	5.2.4	Not applicable
87h	Auto Config Status (AutoCfg Status)	11.10	Section 11.10.1
90h	VRD Over Temperature (VRD Hot)	5.2.5	Section 5.2.5.3
91h-93h	NVMe Therm Mgn	5.2.7.1	Section 5.2.7.1
94h-96h	NVMe Crit Warn	5.2.7.2	Section 5.2.7.2
A0h	Power Supply 1 Fan Tachometer 1 (PS1 Fan Tach 1)	4.5.5	Section 4.5.5.1
A1h	Power Supply 1 Fan Tachometer 2 (PS1 Fan Tach 2)	4.5.5	Section 4.5.5.1
A2h	Intel® Xeon Phi™ Coprocessor Status 1 (GPGPU 1 Status)	11.9.2	Section 11.9.2.1
A3h	Intel® Xeon Phi™ Coprocessor Status 2 (GPGPU 2 Status)	11.9.2	Section 11.9.2.1
A4h	Power Supply 2 Fan Tachometer 1 (PS2 Fan Tach 1)	4.5.5	Section 4.5.5.1
A5h	Power Supply 2 Fan Tachometer 2 (PS3 Fan Tach 2)	4.5.5	Section 4.5.5.1
A8h	Power Supply 3 Fan Tachometer 1 (PS3 Fan Tach 1)	4.5.5	Section 4.5.5.1
A9h	Power Supply 3 Fan Tachometer 2 (PS2 Fan Tach 2)	4.5.5	Section 4.5.5.1
A6h	Intel® Xeon Phi™ Coprocessor Status 3 (GPGPU 3 Status)	11.9.2	Section 11.9.2.1
A7h	Intel® Xeon Phi™ Coprocessor Status 4 (GPGPU 4 Status)	11.9.2	Section 11.9.2.1

Sensor #	Sensor Name	Details Section	Next Steps
B0h	Processor 1 DIMM Aggregate Thermal Margin 1 (P1 DIMM Thrm Mrgn1)	5.2.2	Table 49
B1h	Processor 1 DIMM Aggregate Thermal Margin 2 (P1 DIMM Thrm Mrgn2)	5.2.2	Table 49
B2h	Processor 2 DIMM Aggregate Thermal Margin 1 (P2 DIMM Thrm Mrgn1)	5.2.2	Table 49
B3h	Processor 2 DIMM Aggregate Thermal Margin 2 (P2 DIMM Thrm Mrgn2)	5.2.2	Table 49
B4h	Processor 3 DIMM Aggregate Thermal Margin 1 (P3 DIMM Thrm Mrgn1)	5.2.2	Table 49
B5h	Processor 3 DIMM Aggregate Thermal Margin 2 (P3 DIMM Thrm Mrgn2)	5.2.2	Table 49
B6h	Processor 4 DIMM Aggregate Thermal Margin 1 (P4 DIMM Thrm Mrgn1)	5.2.2	Table 49
B7h	Processor 4 DIMM Aggregate Thermal Margin 2 (P4 DIMM Thrm Mrgn2)	5.2.2	Table 49
B8h	Node Auto-Shutdown Sensor (Auto Shutdown)	4.4.3	Section 4.4.3.1
Bah-BFh	Fan Tachometer Sensors (Chassis specific sensor names)	5.1.1	Table 39
C0h-C3h	Processor 1–4 DIMM Thermal Trip (P1-P4 Mem Thrm Trip)	5.2.6	Section 5.2.6.1
C4h	Intel® Xeon Phi™ Coprocessor Thermal Margin 1 (GPGPU 1 Margin)	11.9.1	Not applicable
C5h	Intel® Xeon Phi™ Coprocessor Thermal Margin 2 (GPGPU 2 Margin)	11.9.1	Not applicable
C6h	Intel® Xeon Phi™ Coprocessor Thermal Margin 3 (GPGPU 3 Margin)	11.9.1	Not applicable
C7h	Intel® Xeon Phi™ Coprocessor Thermal Margin 4 (GPGPU 4 Margin)	11.9.1	Not applicable
C8h-CFh	Global Aggregate Temperature Margin 1–8 (Agg Therm Mrgn 1–8)	5.2.2	Table 49
D0h	Baseboard +12V (BB +12.0V)	4.1	Table 13
D1h	Voltage Fault (Voltage Fault)	4.2	Table 14
D5h	Baseboard Temperature 7 (Platform Specific)	5.2.1	Table 46
D6h	Baseboard Temperature 8 (Platform Specific)	5.2.1	Table 46
D7h	Bad Use PWD	11.11	Section 11.11
DAh	KCS Policy	11.14	Section 11.14
DB	Remote Debug	11.12	Section 11.12
DEh	Baseboard CMOS Battery (BB +3.3V Vbat)	4.1	Table 13
E0h	Hot-swap Backplane 4 Temperature (HSBP 4 Temp)	12.1	Table 117
E2h-E3h	Rear Hard Disk Drive 0 -1 Status (Rear HDD 0–1 Stat)	12.2	Table 119
F0h-FEh	Hard Disk Drive 0–14 Status (HDD 0–14 Status)	12.2	Table 119

3.2 BIOS POST-Owned Sensors (GID = 0001h)

The following table can be used to find the details of sensors owned by BIOS POST.

Table 6. BIOS POST owned sensors

Sensor #	Sensor Name	Details Section	Next Steps
02h	Memory RAS Configuration Status	7.1	Table 68
06h	POST Error	9.1	Section 9.1.1
09h	Intel UPI Link Width Reduced	6.5.1	Section 6.5.1.1
01h	OEM BIOS POST Event	9.3	Not applicable
12h	Memory RAS Mode Select	7.2	Not applicable
83h	OOB Firmware update	11.15	Not applicable
83h	OOB BIOS Configuration	11.16	Not applicable

3.3 BIOS SMI Handler-Owned Sensors (GID = 0033h)

The following table can be used to find the details of sensors owned by BIOS System Management Interrupt (SMI) Handler.

Table 7. BIOS SMI Handler owned sensors

Sensor #	Sensor Name	Details Section	Next Steps
01h	Mirroring Redundancy State	7.3	Section 7.3.1
02h	Memory ECC Error	7.5.1	Table 77
03h	Legacy PCI Error	8.1	Section 8.1.1
04h	PCI Express Fatal Error	8.2.1	Section 8.2.1.1
05h	PCI Express Correctable Error	8.2.2	Section 8.2.2.1
06h	Intel UPI Correctable Error	6.5.2	Section 6.5.2.1
10h	Memory Error Extension	7.6	Not applicable
11h	Sparing Redundancy State	7.4	Section 7.4.1
13h	Memory Parity Error	7.5.2	Section 7.5.2.1
14h	PCI Express Fatal Error#2 (continuation of Sensor 04h)	8.2.1	Section 8.2.1.1
15h	BIOS Recovery Start	9.2	Not applicable
15h	BIOS Recovery Completion	9.2	Not applicable
20h	ADDDC error	7.7	Not applicable

3.4 Intel® NM/Intel® ME Firmware-Owned Sensors (GID = 002Ch or 602Ch)

The following table can be used to find the details of sensors owned by the Intel® Node Manager (Intel® NM)/Intel® Management Engine (Intel® ME) firmware.

Table 8. Intel® Management Engine firmware-owned sensors

Sensor #	Sensor Name	Details Section	Next Steps
17h	Intel® ME Firmware Health Events	13.1	Section 13.1.1
18h	Intel® Node Manager Exception Events	13.2	Section 13.2.1
19h	Intel Node Manager Health Events	13.3	Section 13.3.1
1Ah	Intel Node Manager Operational Capabilities Change Events	13.4	Section 13.4.1
1Bh	Intel Node Manager Alert Threshold Exceeded Events	13.5	Section 13.5.1
B2h	Intel Node Manager SmaRT/CLST Events	13.6	Section 13.6.1

3.5 System Management Software-Owned Events (GID = 0041h)

The following table can be used to find the details of records that are owned by the system management software.

Table 9. System Management Software-owned events

Sensor Name	Record Type	Sensor Type	Details Section	Next Steps
Boot Event	02h	1Fh = Operating system Boot	Table 129	Not applicable
	DCh	Not applicable	Table 130	Not applicable
Shutdown Event	02h	20h = Operating system Stop/Shutdown	Table 131	Not applicable
	DDh	Not applicable	Table 132, Table 133	Not applicable
Bug Check/ Blue Screen	02h	20h = Operating system Stop/Shutdown	Table 134	Not applicable
	DEh	Not applicable	Table 135	Not applicable.

3.6 Linux* Kernel Panic Events (GID = 0021h)

The following table can be used to find the details of records that can be generated when there is a Linux* Kernel panic.

Table 10. Linux* Kernel panic events

Sensor Name	Record Type	Sensor Type	Details Section	Next Steps
Linux* Kernel Panic	02h	20h = Operating system Stop/Shutdown	Table 136	Not applicable
	F0h	Not applicable	Table 137	Not applicable

4. Power Subsystems

The BMC monitors the power subsystem including power supplies, select onboard voltages, and related sensors.

4.1 Threshold-Based Voltage Sensors

The BMC monitors the main voltage sources in the system, including the baseboard, memory, and processors, using IPMI-compliant analog/threshold sensors. Some voltages are only on specific platforms. For details check the platform *Technical Product Specification (TPS)*.

Note: A voltage error can be caused by the device supplying the voltage or by the device using the voltage. For each sensor, it is noted who is supplying the voltage and who is using it.

Table 11. Threshold-based voltage sensors typical characteristics

Byte	Field	Description
11	Sensor Type	02h = Voltage
12	Sensor Number	See Table 13
13	Event Direction and Event Type	[7] Event direction 0b = Assertion Event 1b = Deassertion Event [6:0] Event Type = 01h (Threshold)
14	Event Data 1	[7:6] – 01b = Trigger reading in Event Data 2 [5:4] – 01b = Trigger threshold in Event Data 3 [3:0] – Event Triggers as described in Table 12
15	Event Data 2	Reading that triggered event
16	Event Data 3	Threshold value that triggered event

The following table describes the severity of each of the event triggers for both assertion and deassertion.

Table 12. Threshold-based voltage sensors event triggers

Event Trigger		Assertion Severity	Deassertion Severity	Description
00h	Lower non-critical going low	Degraded	OK	The voltage has dropped below its lower non-critical threshold.
02h	Lower critical going low	Non-fatal	Degraded	The voltage has dropped below its lower critical threshold.
07h	Upper non-critical going high	Degraded	OK	The voltage has gone over its upper non-critical threshold.
09h	Upper critical going high	Non-fatal	Degraded	The voltage has gone over its upper critical threshold.

Table 13. Threshold-based voltage sensors – next steps

Sensor #	Sensor Name	Next Steps
D0h	Baseboard +12V (BB +12.0V)	+12 V is supplied by the power supplies. +12 V is used by SATA drives, fans, and PCIe cards. In addition, it is used to generate various processor voltages. 1. Ensure that all cables are connected correctly. 2. Check connections on the fans and HDDs. 3. If the issue follows the component, swap it, otherwise, replace the board. 4. If the issue remains, replace the power supplies.
D1h	Aggregate Voltage Fault Sensor	The voltages in this sensor are all derived on the server board from the 12 V or 3.3 V power. 1. Remove all but minimum components for operation and check sensor. 2. Inspect for contamination in connectors (DIMMS, PCIe). 3. If error remains, replace the board.
DEh	Baseboard CMOS Battery (BB +3.3V Vbat)	Vbat is supplied by the CMOS battery when AC power is off (Battery Voltage is 3.0 V) and by the main board when AC power is on (Battery Voltage is 3.3 V). Vbat is used by the CMOS and related circuits. 1. Replace the CMOS battery. Any battery of type CR2032 can be used. 2. If error remains (unlikely), replace the board.

4.2 Aggregate Voltage Fault Sensor

The discrete voltage sensor monitors multiple voltages from sensors around the baseboard and then asserts a bit in the SEL event data for each sensor that is out of range. The Voltage name for the asserted bit can be retrieved using the Get Voltage Name IPMI function. For details, check *BMC External Product Specification (EPS)*.

Table 14. Aggregate voltage sensors typical characteristics for S7200AP/S7200APR, S1200SP, S2600WT/S2600WTR, S2600CW/S2600CWR, S2600KP/S2600KPR, S2600TP/S2600TPR

Byte	Field	Description
11	Sensor Type	02h = Voltage
12	Sensor Number	D1h
13	Event Direction and Event Type	[7] Event direction 0b = Assertion Event 1b = Deassertion Event [6:0] Event Type = 01h A1 = Event asserted
14	Event Data 1	[7:6] – 10b = Trigger reading in Event Data 2 [5:4] – 10b = Trigger threshold in Event Data 3 [3:0] – 0001b = OEM Event Trigger
15	Event Data 2	Sensor Number from Table 18 or Table 19 Lower Bytes (0 -7)
16	Event Data 3	Sensor Number from Table 18 or Table 19 Upper Bytes (8 to 15)
17	Extended Data 1	Byte 1: [7:4] = Number of valid extended data bytes following [3:2] = Reserved [1:0] Severity = Severity status. 0x01: Severity Non-Critical 0x02: Severity Critical
18	Extended Data 2	Reserved 0x00
19	Extended Data 3	Reserved 0x00
20	Extended Data 4	Direction of Assertion (Lower Sen 0–7) Bit Mapped in ED2: 1 = Higher Bit Mapped in ED2: 0 = Lower
21	Extended Data 5	Direction of Assertion (Higher Sen 8–15) Bit Mapped in ED3: 1 = Higher Bit Mapped in ED3: 0 = Lower
22	Extended Data 6	Reserved 0x00
23	Extended Data 7	Reserved 0x00
24	Extended Data 8	Not used 0xFF

Table 15. Aggregate voltage sensors typical characteristics for S2600BP/S2600BPR, S2600WF/S2600WFR, S2600ST/S2600STR

Byte	Field	Description
11	Sensor Type	02h = Voltage
12	Sensor Number	D1h
13	Event Direction and Event Type	[7] Event direction 0b = Assertion Event 1b = Deassertion Event [6:0] Event Type = 01h A1 = Event asserted
14	Event Data 1	[7:6] – 10b = Trigger reading in Event Data 2 [5:4] – 10b = Trigger threshold in Event Data 3 [3:0] – 0001b = OEM Event Trigger
15	Event Data 2	Voltage Fault Status [Bit 0] = Not Used [Bit 1] = +3.3V [Bit 2] = VNN PCH Aux [Bit 3] = +1.05V PCH Aux [Bit 4] = +0.83V LAN Aux [Bit 5] = 12V Aux [Bit 6] = +1.8V PCH Aux [Bit 7] = VCC In CPU0
16	Event Data 3	Voltage Fault Status [Bit 0] = VCC In CPU1 [Bit 1] = VDDQ ABC CPU0 [Bit 2] = VDDQ DEF CPU0 [Bit 3] = VDDQ ABC CPU1 [Bit 4] = VDDQ DEF CPU1 [Bit 5] = VCCIO CPU0 [Bit 6] = VCCIO CPU1 [Bit 7] = Not Used
17	Extended Data 1	[7] - Reserved [6:4] - 110b = Extended SEL record length of 6 bytes [3:2] - Reserved [1:0] - Severity Status 10b = Severity Critical
18	Extended Data 2	Voltage Fault Status = Not Used
19	Extended Data 3	Voltage Fault Status = Not Used
20	Extended Data 4	Upper Non-Critical Voltage Fault Status [Bit 0] = Not Used [Bit 1] = +3.3V [Bit 2] = VNN PCH Aux [Bit 3] = +1.05V PCH Aux [Bit 4] = +0.83V LAN Aux [Bit 5] = 12V Aux [Bit 6] = +1.8V PCH Aux [Bit 7] = VCC In CPU0
21	Extended Data 5	Upper Non-Critical Voltage Fault Status [Bit 0] = VCC In CPU1 [Bit 1] = VDDQ ABC CPU0 [Bit 2] = VDDQ DEF CPU0 [Bit 3] = VDDQ ABC CPU1 [Bit 4] = VDDQ DEF CPU1 [Bit 5] = VCCIO CPU0 [Bit 6] = VCCIO CPU1 [Bit 7] = Not Used

Byte	Field	Description
22	Extended Data 6	Lower Non-Critical Voltage Fault Status [Bit 0] = Not Used [Bit 1] = +3.3V [Bit 2] = VNN PCH Aux [Bit 3] = +1.05V PCH Aux [Bit 4] = +0.83V LAN Aux [Bit 5] = 12V Aux [Bit 6] = +1.8V PCH Aux [Bit 7] = VCC In CPU0
23	Extended Data 7	Lower Non-Critical Voltage Fault Status [Bit 0] = VCC In CPU1 [Bit 1] = VDDQ ABC CPU0 [Bit 2] = VDDQ DEF CPU0 [Bit 3] = VDDQ ABC CPU1 [Bit 4] = VDDQ DEF CPU1 [Bit 5] = VCCIO CPU0 [Bit 6] = VCCIO CPU1 [Bit 7] = Not Used
24	Extended Data 8	Not used `0xFF`

There are two types of voltage fault sensors in S9200WK that monitor all voltage: voltage fault and Max11617 voltage fault. The two aggregate sensors state provided reflects whether any of the monitored voltages has crossed an associated non-critical threshold. Both assertion and de-assertion event generation are supported. An OEM bitmap code is written into the SEL event data bytes to indicate which voltages are exhibiting the fault condition and a separate bit-map to indicate which non-critical threshold was crossed (upper or lower). The sensor goes to a deasserted state only when all voltages have returned to below their non-critical thresholds. The following is SEL event data definition.

Table 16. Aggregate voltage sensors typical characteristics for S9200WK

Byte	Field	Description
11	Sensor Type	`02h` = Voltage
12	Sensor Number	`D1h`
13	Event Direction and Event Type	[7] Event direction `0b` = Assertion Event `1b` = Deassertion Event [6:0] Event Type = 01h `A1` = Event asserted
14	Event Data 1	[7:6] – `10b` = Trigger reading in Event Data 2 [5:4] – `10b` = Trigger threshold in Event Data 3 [3:0] – `0001b` = OEM Event Trigger
15	Event Data 2	Voltage Fault Status [Bit 0] = Not Used [Bit 1] = Not Used [Bit 2] = VNN PCH Aux [Bit 3] = +1.05V PCH Aux [Bit 4] = +5.0V Aux [Bit 5] = 12V Aux [Bit 6] = +1.8V PCH Aux [Bit 7] = Not Used

Byte	Field	Description
16	Event Data 3	Voltage Fault Status [Bit 0] = VCC In CPU0 [Bit 1] = VCC In CPU1 [Bit 2] = VDDQ ABC CPU0 [Bit 3] = VDDQ DEF CPU0 [Bit 4] = VDDQ ABC CPU1 [Bit 5] = VDDQ DEF CPU1 [Bit 6] = VCCIO CPU0 [Bit 7] = VCCIO CPU1
17	Extended Data 1	[7] - Reserved [6:4] - 110b = Extended SEL record length of 6 bytes [3:2] - Reserved [1:0] - Severity Status 10b = Severity Critical
18	Extended Data 2	Voltage Fault Status = Not Used
19	Extended Data 3	Voltage Fault Status = Not Used
20	Extended Data 4	Upper Non-Critical Voltage Fault Status [Bit 0] = Not Used [Bit 1] = Not Used [Bit 2] = VNN PCH Aux [Bit 3] = +1.05V PCH Aux [Bit 4] = +5.0V Aux [Bit 5] = 12V Aux [Bit 6] = +1.8V PCH Aux [Bit 7] = Not Used
21	Extended Data 5	Upper Non-Critical Voltage Fault Status [Bit 0] = VCC In CPU0 [Bit 1] = VCC In CPU1 [Bit 2] = VDDQ ABC CPU0 [Bit 3] = VDDQ DEF CPU0 [Bit 4] = VDDQ ABC CPU1 [Bit 5] = VDDQ DEF CPU1 [Bit 6] = VCCIO CPU0 [Bit 7] = VCCIO CPU1
22	Extended Data 6	Lower Non-Critical Voltage Fault Status [Bit 0] = Not Used [Bit 1] = Not Used [Bit 2] = VNN PCH Aux [Bit 3] = +1.05V PCH Aux [Bit 4] = +5.0V Aux [Bit 5] = 12V Aux [Bit 6] = +1.8V PCH Aux [Bit 7] = Not Used
23	Extended Data 7	Lower Non-Critical Voltage Fault Status [Bit 0] = VCC In CPU0 [Bit 1] = VCC In CPU1 [Bit 2] = VDDQ ABC CPU0 [Bit 3] = VDDQ DEF CPU0 [Bit 4] = VDDQ ABC CPU1 [Bit 5] = VDDQ DEF CPU1 [Bit 6] = VCCIO CPU0 [Bit 7] = VCCIO CPU1
24	Extended Data 8	Not used `0xFF`

Table 17. Aggregate voltage sensors typical characteristics for Max11617

Byte	Field	Description
11	Sensor Type	02h = Voltage
12	Sensor Number	D2h
13	Event Direction and Event Type	[7] Event direction 0b = Assertion Event 1b = Deassertion Event [6:0] Event Type = 01h A1 = Event asserted
14	Event Data 1	[7:6] – 10b = Trigger reading in Event Data 2 [5:4] – 10b = Trigger threshold in Event Data 3 [3:0] – 0001b = OEM Event Trigger
15	Event Data 2	Voltage Fault Status [Bit 0] = Not Used [Bit 1] = PVCCIN CPU0 D1 [Bit 2] = PVCCIN CPU1 D1 [Bit 3] = PVCCSA CPU0 D0 [Bit 4] = PVCCSA CPU0 D1 [Bit 5] = PVCCSA CPU1 D0 [Bit 6] = PVCCSA CPU1 D1 [Bit 7] = PVCCIO CPU0 D1
16	Event Data 3	Voltage Fault Status [Bit 0] = PVCCIO CPU1 D1 [Bit 1] = PVPP ABC CPU0 [Bit 2] = PVPP DEF CPU0 [Bit 3] = PVPP ABC CPU1 [Bit 4] = PVPP DEF CPU1 [Bit 5] = Not Used [Bit 6] = Not Used [Bit 7] = Not Used
17	Extended Data 1	[7] - Reserved [6:4] - 110b = Extended SEL record length of 6 bytes [3:2] - Reserved [1:0] - Severity Status 10b = Severity Critical
18	Extended Data 2	Voltage Fault Status = Not Used
19	Extended Data 3	Voltage Fault Status = Not Used
20	Extended Data 4	Upper Non-Critical Voltage Fault Status [Bit 0] = Not Used [Bit 1] = PVCCIN CPU0 D1 [Bit 2] = PVCCIN CPU1 D1 [Bit 3] = PVCCSA CPU0 D0 [Bit 4] = PVCCSA CPU0 D1 [Bit 5] = PVCCSA CPU1 D0 [Bit 6] = PVCCSA CPU1 D1 [Bit 7] = PVCCIO CPU0 D1
21	Extended Data 5	Upper Non-Critical Voltage Fault Status [Bit 0] = PVCCIO CPU1 D1 [Bit 1] = PVPP ABC CPU0 [Bit 2] = PVPP DEF CPU0 [Bit 3] = PVPP ABC CPU1 [Bit 4] = PVPP DEF CPU1 [Bit 5] = Not Used [Bit 6] = Not Used [Bit 7] = Not Used

Byte	Field	Description
22	Extended Data 6	Lower Non-Critical Voltage Fault Status [Bit 0] = Not Used [Bit 1] = PVCCIN CPU0 D1 [Bit 2] = PVCCIN CPU1 D1 [Bit 3] = PVCCSA CPU0 D0 [Bit 4] = PVCCSA CPU0 D1 [Bit 5] = PVCCSA CPU1 D0 [Bit 6] = PVCCSA CPU1 D1 [Bit 7] = PVCCIO CPU0 D1
23	Extended Data 7	Lower Non-Critical Voltage Fault Status [Bit 0] = PVCCIO CPU1 D1 [Bit 1] = PVPP ABC CPU0 [Bit 2] = PVPP DEF CPU0 [Bit 3] = PVPP ABC CPU1 [Bit 4] = PVPP DEF CPU1 [Bit 5] = Not Used [Bit 6] = Not Used [Bit 7] = Not Used
24	Extended Data 8	Not used `0xFF`

Table 18. Aggregate voltage sensors mappings - 1

	S7200AP			S1200SP			S2600WT		
		Upper	Lower		Upper	Lower		Upper	Lower
ED2[0]	BB CPU CORE	1.006	0.723				BB 1.8V P1 VCC	1.905	1.435
ED2[1]	BB 0.95V VCCU	0.989	0.911	BB 5V	5.457	4.562	BB 1.8V P2 VCC	1.905	1.435
ED2[2]	BB 1.2V VCCD	1.25	1.171	BB 3.3V	3.587	3.025	BB 1.2V P1DDR AB	1.296	1.107
ED2[3]	BB 1.2V VCCMP	1.235	1.138	BB 5V STBY	5.457	4.562	BB 1.2V P1DDR CD	1.296	1.107
ED2[4]	BB 0.75V VCCCLR	0.88	0.676	BB 2.5V VPP	2.837	2.334	BB 1.2V P2DDR EF	1.296	1.107
ED2[5]	BB 0.95V VCCMLB	0.989	0.911	BB 3V3 AUX	3.587	3.025	BB 1.2V P2DDR GH	1.296	1.107
ED2[6]	BB 2.5V VPP MEM	2.694	2.435	BB PVVC VCCIO	1.027	0.876	BB 2.62V VPP	2.968	2.407
ED2[7]	BB 1.0V VCCPIO	1.034	0.967	BB P1V0 PCH	1.08	0.942	BB 1.05V VCC IO	1.113	0.989
ED3[0]	BB 1.5V PCH	1.571	1.43	BB P1V2 VDDQ	1.296	1.107	BB 1.5V PCH	1.619	1.385
ED3[1]	BB 1.05V PCH	1.101	1	PVCC_VCCSA	1.08	0.942	BB 1.05V PCH	1.134	0.968
ED3[2]	BB 1.05V STBY	1.101	1				BB 1.05V ASW PCH	1.134	0.968
ED3[3]	BB 5.0V	5.322	4.688	BB 12.0V 1	13.158	10.894	BB 1.0V AUX LAN	1.08	0.895
ED3[4]	BB 0.9 VCCCDCORE	0.944	0.857				BB 3.3V AUX	3.45	3.152
ED3[5]	BB 3.3V	3.498	3.108	BB PVCC_GTS	1.542	-0.003	BB 12V AUX	12.782	10.894
ED3[6]				BB PVCC CPU	1.563	-0.003			
ED3[7]									

Table 19. Aggregate voltage sensors mappings - 2

	S2600CW	S2600CWT		S2600CWTS		S2600CW2		S2600CW2S	
		Upper	Lower	Upper	Lower	Upper	Lower	Upper	Lower
ED2[0]	BB 1.8V P1 VCC	1.905	1.435	1.905	1.435	1.905	1.435	1.905	1.435
ED2[1]	BB 1.8V P2 VCC	1.905	1.435	1.905	1.435	1.905	1.435	1.905	1.435
ED2[2]	BB 1.2V P1DDR AB	1.296	1.107	1.296	1.107	1.296	1.107	1.296	1.107
ED2[3]	BB 1.2V P1DDR CD	1.296	1.107	1.296	1.107	1.296	1.107	1.296	1.107
ED2[4]	BB 1.2V P2DDR EF	1.296	1.107	1.296	1.107	1.296	1.107	1.296	1.107
ED2[5]	BB 1.2V P2DDR GH	1.296	1.107	1.296	1.107	1.296	1.107	1.296	1.107
ED2[6]	BB 2.62V VPP	2.833	2.331	2.833	2.331	2.833	2.331	2.833	2.331
ED2[7]	BB 1.05V VCC IO	1.134	0.968	1.134	0.968	1.134	0.968	1.134	0.968
ED3[0]	BB 1.5V PCH	1.619	1.385	1.619	1.385	1.619	1.385	1.619	1.385
ED3[1]	BB 1.05V PCH	1.134	0.968	1.134	0.968	1.134	0.968	1.134	0.968
ED3[2]	BB 1.05V ASW PCH	1.134	0.968	1.134	0.968	1.134	0.968	1.134	0.968
ED3[3]	BB 1.0V AUX LAN	0.865	0.737	0.919	0.783	1.08	0.922	1.08	0.7
ED3[4]	BB 3.3V AUX	3.587	3.025	3.587	3.025	3.587	3.025	3.587	3.025
ED3[5]									
ED3[6]	BB 3.3V	3.587	3.025	3.587	3.025	3.587	3.025	3.587	3.025
ED3[7]									

Table 20. Aggregate voltage sensors mappings - 3

	S2600KPF			**S2600KP**		**S2600TP**	**S2600TPF**		**S2600TP**	
		Upper	Lower	Upper	Lower		Upper	Lower	Upper	Lower
ED2[0]	BB 1.8V P1 VCC	1.905	1.435	1.905	1.435	BB 1.8V P1 VCC	1.905	1.435	1.905	1.435
ED2[1]	BB 1.8V P2 VCC	1.905	1.435	1.905	1.435	BB 1.8V P2 VCC	1.905	1.435	1.905	1.435
ED2[2]	BB 1.2V P1DDR AB	1.296	1.107	1.296	1.107	BB 1.2V P1DDR AB	1.296	1.107	1.296	1.107
ED2[3]	BB 1.2V P1DDR CD	1.296	1.107	1.296	1.107	BB 1.2V P1DDR CD	1.296	1.107	1.296	1.107
ED2[4]	BB 1.2V P2DDR EF	1.296	1.107	1.296	1.107	BB 1.2V P2DDR EF	1.296	1.107	1.296	1.107
ED2[5]	BB 1.2V P2DDR GH	1.296	1.107	1.296	1.107	BB 1.2V P2DDR GH	1.296	1.107	1.296	1.107
ED2[6]	BB 2.62V VPP	2.833	2.331	2.833	2.331	BB 2.62V VPP	2.833	2.331	2.833	2.331
ED2[7]	BB 1.05V VCC IO	1.134	0.968	1.134	0.968	BB 1.05V VCC IO	1.134	0.968	1.134	0.968
ED3[0]	BB 1.5V PCH	1.619	1.385	1.619	1.385	BB 1.5V PCH	1.619	1.385	1.619	1.385
ED3[1]	BB 1.05V PCH	1.134	0.968	1.134	0.968	BB 1.05V PCH	1.134	0.968	1.134	0.968
ED3[2]	BB 0.9V IB CORE	1.065	0.83			BB 0.9V IB CORE	1.065	0.83		
ED3[3]	BB 5V AUX	5.457	4.562	5.457	4.562	BB 5V AUX	5.457	4.562	5.457	4.562
ED3[4]	BB 1.0V AUX	1.039	0.961	1.039	0.961	BB 1.0V AUX	1.039	0.961	1.039	0.961
ED3[5]	BB 3.3V	3.587	3.025	3.587	3.025	BB 3.3V	3.587	3.025	3.587	3.025
ED3[6]										
ED3[7]										

Table 21. Aggregate voltage sensors mappings – 4

	S2600WF/ S2600ST			S2600BP			S2600BT		
		Upper	Lower		Upper	Lower		Upper	Lower
ED2[0]									
ED2[1]	BB 3.3V	3.541	3.066	BB 3.3V	3.541	3.066	BB 3.3V	3.541	3.066
ED2[2]	VNN PCH Aux	1.049	0.807	VNN PCH Aux	1.049	0.807	VNN PCH Aux	1.049	0.807
ED2[3]	BB 1.05V PCH Aux	1.106	0.995	BB 1.05V PCH Aux	1.106	0.995	BB 1.05V PCH Aux	1.106	0.995
ED2[4]	BB 0.83V LAN Aux	0.875	0.786	BB 0.83V LAN Aux	0.875	0.786			
ED2[5]	BB 12V Aux	13.101	10.945	BB 5.0V Aux	5.442	4.576	BB 12V Aux	13.101	10.945
ED2[6]	BB 1.8V PCH Aux	1.904	1.699	BB 1.8V PCH Aux	1.904	1.699	BB 1.8V PCH Aux	1.904	1.699
ED2[7]	VCC In CPU0	2.088	1.418	VCC In CPU0	2.088	1.418	VCC In CPU0	2.088	1.418
ED3[0]	VCC In CPU1	2.088	1.418	VCC In CPU1	2.088	1.418	VCC In CPU1	2.088	1.418
ED3[1]	VDDQ ABC CPU0	1.263	1.138	VDDQ ABC CPU0	1.263	1.138	VDDQ ABC CPU0	1.263	1.138
ED3[2]	VDDQ DEF CPU0	1.263	1.138	VDDQ DEF CPU0	1.263	1.138	VDDQ DEF CPU0	1.263	1.138
ED3[3]	VDDQ ABC CPU1	1.263	1.138	VDDQ ABC CPU1	1.263	1.138	VDDQ ABC CPU1	1.263	1.138
ED3[4]	VDDQ DEF CPU1	1.263	1.138	VDDQ DEF CPU1	1.263	1.138	VDDQ DEF CPU1	1.263	1.138
ED3[5]	VCCIO CPU0	1.155	0.752	VCCIO CPU0	1.155	0.752	VCCIO CPU0	1.155	0.752
ED3[6]	VCCIO CPU1	1.155	0.752	VCCIO CPU1	1.155	0.752	VCCIO CPU1	1.155	0.752
ED3[7]									

Table 22. Discrete voltage sensors – next steps

Voltage Name	Next Steps
BB 1.8V P1 VCC	This 1.8 V line is supplied by the main board. This 1.8 V line is used by processor 1. 1. Ensure that all cables are connected correctly. 2. Check that the processor is seated properly. 3. Cross test the processors. If the issue remains with the processor socket, replace the main board, otherwise the processor.
BB 1.8V P2 VCC	This 1.8 V line is supplied by the main board. This 1.8 V line is used by processor 2. 1. Ensure that all cables are connected correctly. 2. Check that the processor is seated properly. 3. Cross test the processors. If the issue remains with the processor socket, replace the main board, otherwise the processor.
BB 1.2V P1DDR AB	This 1.2 V line is supplied by the main board. This 1.2 V line is used by processor 1 memory slots A and B. 1. Ensure that all cables are connected correctly. 2. Check the DIMMs are seated properly. 3. Cross test the DIMMs. If the issue remains with the DIMMs on this socket, replace the main board, otherwise the DIMM.
BB 1.2V P1DDR CD	This 1.2 V line is supplied by the main board. This 1.2 V line is used by processor 1 memory slots C and D. 1. Ensure that all cables are connected correctly. 2. Check the DIMMs are seated properly. 3. Cross test the DIMMs. If the issue remains with the DIMMs on this socket, replace the main board, otherwise the DIMM.

Voltage Name	Next Steps
BB 1.2V P2DDR EF	This 1.2 V line is supplied by the main board. This 1.2 V line is used by processor 2 memory slots E and F. 1. Ensure that all cables are connected correctly. 2. Check the DIMMs are seated properly. 3. Cross test the DIMMs. If the issue remains with the DIMMs on this socket, replace the main board, otherwise the DIMM.
BB 1.2V P2DDR GH	This 1.2 V line is supplied by the main board. This 1.2 V line is used by processor 2 memory slots G and H. 1. Ensure that all cables are connected correctly. 2. Check the DIMMs are seated properly. 3. Cross test the DIMMs. If the issue remains with the DIMMs on this socket, replace the main board, otherwise the DIMM.
BB 2.62V VPP	This 2.62 V line is supplied by the main board. This 2.62 V line is used by memory. 1. Ensure that all cables are connected correctly. 2. Check the DIMMs are seated properly. 3. Cross test the DIMMs. If the issue remains with the DIMMs on special socket, replace the main board, otherwise the DIMM.
BB 1.05V VCC IO	This 1.05 V line is supplied by the main board. This 1.05 V line is used by processor and PECI. 1. Ensure that all cables are connected correctly. 2. Check that the processors are seated properly. 3. Cross test the processors. If the issue remains with the processor on special socket, replace the main board, otherwise the Processor.
BB 1.5V PCH	This 1.5 V line is supplied by the main board. This 1.5 V line is used by PCH. 1. Ensure that all cables are connected correctly. 2. If the issue remains, replace the board.
BB 1.05V PCH	This 1.05 V line is supplied by the main board. This 1.05 V line is used by PCH. 1. Ensure that all cables are connected correctly. 2. If the issue remains, replace the board.
BB 1.05V ASW PCH	This 1.05 V line is supplied by the main board. This 1.05 V line is used by PCH. 1. Ensure that all cables are connected correctly. 2. If the issue remains, replace the board.
BB 0.9V IB CORE	+0.9 V Core IB is supplied by the main board on specific platforms. +0.9 V Core IB is used by the onboard InfiniBand* Technology controller on those specific platforms. 1. Ensure that all cables are connected correctly. 2. If the issue remains, replace the board. 3. If the issue remains, replace the power supplies.
BB 1.0V AUX LAN	+1.0 V AUX LAN is supplied by the main board. +1.0 V AUX LAN is used by onboard NIC Intel® X540. 1. Ensure that all cables are connected correctly. 2. If the issue remains, replace the board. 3. If the issue remains, replace the power supplies.
BB 5V AUX	This 5 V line is supplied by the HSBP (Platform Specific). This 5 V line is used optionally and depends on customer's design. 1. Ensure that all cables are connected correctly. 2. If the issue remains, replace the board.

Voltage Name	Next Steps
BB 3.3V AUX	+3.3 V AUX is supplied by the main board. +3.3 V AUX is used by the BMC, clock chips, PCIe Slot, onboard NIC, PCH. 1. Ensure that all cables are connected correctly. 2. If the issue remains, replace the board. 3. If the issue remains, replace the power supplies.
BB 1.0V AUX	+1.0 V AUX is supplied by the main board. +1.0 V AUX is used by the BMC, onboard NIC. 1. Ensure that all cables are connected correctly. 2. If the issue remains, replace the board. 3. If the issue remains, replace the power supplies.
BB 12V AUX	+12 V AUX is supplied by the Power Supply. +12 V AUX is used by the BMC, clock chips, PCIe Slot, onboard NIC, PCH. 1. Ensure that all cables are connected correctly. 2. If the issue remains, replace the board. 3. If the issue remains, replace the power supplies.
BB 3.3V	+3.3 V is supplied by the power supplies for pedestal systems, and supplied by the main board on rack-optimized systems. +3.3 V is used by the PCIe and PCI-X slots. 1. Ensure that all cables are connected correctly. 2. Reseat any PCIe cards. 3. Try PCIe cards in other PCIe slots. 4. If the issue follows the card, swap it; otherwise, replace the main board. 5. If the issue remains, replace the power supplies.
VNN PCH Aux	This VNN PCH Aux line is supplied by the main board. This VNN PCH Aux line is used by PCH. 1. Ensure that all cables are connected correctly. 2. If the issue remains, replace the board.
BB 1.05V PCH Aux	This 1.05V Aux line is supplied by the main board. This 1.05V Aux line is used by PCH. 1. Ensure that all cables are connected correctly. 2. If the issue remains, replace the board.
BB 0.83V LAN Aux	0.83V LAN AUX is supplied by the main board. 0.83V LAN AUX is used by onboard NIC controller 1. Ensure that all cables are connected correctly. 2. If the issue remains, replace the board. 3. If the issue remains, replace the power supplies.
BB 1.8V PCH Aux	This 1.8V Aux line is supplied by the main board. This 1.8V Aux line is used by PCH. 1. Ensure that all cables are connected correctly. 2. If the issue remains, replace the board.
VCC In CPU0	This 1.8 V line is supplied by the main board. This 1.8 V line is used by processor 1. 1. Ensure that all cables are connected correctly. 2. Check that the processor is seated properly. 3. Cross test the processors. If the issue remains with the processor socket, replace the main board, otherwise the processor.

Voltage Name	Next Steps
VCC In CPU1	This 1.8 V line is supplied by the main board. This 1.8 V line is used by processor 2. 1. Ensure that all cables are connected correctly. 2. Check that the processor is seated properly. 3. Cross test the processors. If the issue remains with the processor socket, replace the main board, otherwise the processor.
VDDQ ABC CPU0	This 1.2 V line is supplied by the main board. This 1.2 V line is used by processor 1 memory slots A/B/C. 1. Ensure that all cables are connected correctly. 2. Check the DIMMs are seated properly. 3. Cross test the DIMMs. If the issue remains with the DIMMs on this socket, replace the main board, otherwise the DIMM.
VDDQ DEF CPU0	This 1.2 V line is supplied by the main board. This 1.2 V line is used by processor 1 memory slots D/E/F. 1. Ensure that all cables are connected correctly. 2. Check the DIMMs are seated properly. 3. Cross test the DIMMs. If the issue remains with the DIMMs on this socket, replace the main board, otherwise the DIMM.
VDDQ ABC CPU1	This 1.2 V line is supplied by the main board. This 1.2 V line is used by processor 2 memory slots A/B/C. 1. Ensure that all cables are connected correctly. 2. Check the DIMMs are seated properly. 3. Cross test the DIMMs. If the issue remains with the DIMMs on this socket, replace the main board, otherwise the DIMM.
VDDQ DEF CPU1	This 1.2 V line is supplied by the main board. This 1.2 V line is used by processor 2 memory slots D/E/F. 1. Ensure that all cables are connected correctly. 2. Check the DIMMs are seated properly. 3. Cross test the DIMMs. If the issue remains with the DIMMs on this socket, replace the main board, otherwise the DIMM.
VCCIO CPU0	This 1.0 V line is supplied by the main board. This 1.0 V line is used by processor and PECI. 1. Ensure that all cables are connected correctly. 2. Check that the processors are seated properly. 3. Cross test the processors. If the issue remains with the processor on special socket, replace the main board, otherwise the Processor.
VCCIO CPU1	This 1.0 V line is supplied by the main board. This 1.0 V line is used by processor and PECI. 1. Ensure that all cables are connected correctly. 2. Check that the processors are seated properly. 3. Cross test the processors. If the issue remains with the processor on special socket, replace the main board, otherwise the Processor.

4.3 Voltage Regulator Watchdog Timer Sensor

The BMC firmware monitors that the power sequence for the board voltage regulator (VR) controllers is completed when a DC power-on is initiated. Incompletion of the sequence indicates a board problem, in which case the firmware powers down the system.

The sequence is as follows:

- BMC firmware monitors the `PowerSupplyPowerGood` signal for assertion, indicating a DC-power-on has been initiated, and starts a timer (VR Watchdog Timer). For platforms based on Intel® Xeon® processor E5 4600/2600/2400/1600 product families, this timeout is 500 ms.
- If the `SystemPowerGood` signal has not asserted by the time the VR Watchdog Timer expires, the firmware powers down the system, logs a SEL entry, and emits a beep code (1-5-1-2). This failure is termed as VR Watchdog Timeout.

Table 23. Voltage regulator watchdog timer sensor typical characteristics

Byte	Field	Description
11	Sensor Type	`02h` = Voltage
12	Sensor Number	`0Bh`
13	Event Direction and Event Type	[7] Event direction `0b` = Assertion Event `1b` = Deassertion Event [6:0] Event Type = 03h (“digital” Discrete)
14	Event Data 1	[7:6] – `00b` = Unspecified Event Data 2 [5:4] – `00b` = Unspecified Event Data 3 [3:0] – Event Trigger Offset = `1h` = State Asserted
15	Event Data 2	Not used
16	Event Data 3	Not used

4.3.1 Voltage Regulator Watchdog Timer Sensor – Next Steps

1. Ensure that all the connectors from the power supply are well seated.
2. Cross test the baseboard. If the issue remains with the baseboard, replace the baseboard.

4.4 Power Unit

The power unit monitors the power state of the system and logs the state changes in the SEL.

4.4.1 Power Unit Status Sensor

The power unit status sensor monitors the power state of the system and logs state changes. Expected power-on events, such as DC ON/OFF, are logged and unexpected events, such as AC loss and power good loss, are also logged.

Table 24. Power unit status sensors typical characteristics

Byte	Field	Description
11	Sensor Type	09h = Power Unit
12	Sensor Number	01h
13	Event Direction and Event Type	[7] Event direction 0b = Assertion Event 1b = Deassertion Event [6:0] Event Type = 6Fh (Sensor Specific)
14	Event Data 1	[7:6] – 00b = Unspecified Event Data 2 [5:4] – 00b = Unspecified Event Data 3 [3:0] = Sensor Specific offset as described in Table 25
15	Event Data 2	Not used
16	Event Data 3	Not used

Table 25. Power unit status sensor – sensor specific offsets – next steps

Sensor Specific Offset		Description	Next Steps
00h	Power down	System is powered down.	Informational event
02h	240 VA power down	240 VA power limit was exceeded and the hardware forced a power down.	This could be caused by many things. 1. If hardware was recently added, try removing it. 2. Remove/replace any add-in adapters. 3. Remove/replace the power supply. 4. Remove/replace the processors, DIMM, and/or hard drives. 5. Remove/replace the boards in the system.
04h	AC Lost	AC power was removed.	Informational event
05h	Soft Power Control Failure	Asserted if the system fails to power on due to the following power control sources: • Chassis Control command • PEF action • BMC Watchdog Timer • Power State Retention	This could be caused by the power supply subsystem or system components. 1. Verify that all power cables and adapters are connected properly (AC cables as well as the cables between the power supply unit (PSU) and system components). 2. Cross test the PSU if possible. 3. Replace the power subsystem.

Sensor Specific Offset		Description	Next Steps
06h	Power Unit Failure	Power subsystem experienced a failure. Asserted for one of the following conditions: • Unexpected de-assertion of system POWER_GOOD signal. • System fails to respond to any power control source's attempt to power down the system. • System fails to respond to any hardware power control source's attempt to power on the system. • Power Distribution Board (PDB) failure is detected (applies only to systems that have a PDB).	Indicates that a power supply failed. 1. Remove and reapply AC power. 2. Verify that all power cables and adapters are connected properly (AC cables as well as the cables between the PSU and system components). 3. Cross test the PSU if possible. 4. If the power supply still fails, replace it. 5. If the problems persist, replace the baseboard.

4.4.2 Power Unit Redundancy Sensor

This sensor is enabled on the systems that support redundant power supplies. When a system has AC applied or if it loses redundancy of the power supplies, a message is logged into the SEL.

Table 26. Power Unit redundancy sensors typical characteristics

Byte	Field	Description
11	Sensor Type	09h = Power Unit
12	Sensor Number	02h
13	Event Direction and Event Type	[7] Event direction 0b = Assertion Event 1b = Deassertion Event [6:0] Event Type = 0Bh (Generic Discrete)
14	Event Data 1	[7:6] – 00b = Unspecified Event Data 2 [5:4] – 00b = Unspecified Event Data 3 [3:0] – Event Trigger Offset as described in Table 27
15	Event Data 2	Not used
16	Event Data 3	Not used

Table 27. Power unit redundancy sensor – event trigger offset – next steps

Event Trigger Offset		Description	Next Steps
00h	Fully redundant	System is fully operational.	Informational Event
01h	Redundancy lost	System is not running in redundant power supply mode.	This event is accompanied by specific power supply errors (AC lost, PSU failure, and so on). Troubleshoot these events accordingly.
02h	Redundancy degraded		
03h	Non-redundant, sufficient from redundant		
04h	Non-redundant, sufficient from insufficient		
05h	Non-redundant, insufficient		
06h	Non-redundant, degraded from fully redundant		
07h	Redundant, degraded from non-redundant		

4.4.3 Node Auto Shutdown Sensor

The BMC supports a Node Auto Shutdown sensor for logging an SEL event due to an emergency shutdown of a node due to loss of power supply redundancy or PSU CLST throttling due to an overcurrent warning condition. This sensor is applicable only to multi-node systems.

The sensor is rearmed on power-on (AC or DC power-on transitions).

This sensor is only used for triggering SEL to indicate node or power auto shutdown assertion or deassertion.

Table 28. Node auto shutdown sensor typical characteristics

Byte	Field	Description
11	Sensor Type	09h = Power Unit
12	Sensor Number	B8h
13	Event Direction and Event Type	[7] Event direction 0b = Assertion Event 1b = Deassertion Event [6:0] Event Type = 03h (“digital” discrete)
14	Event Data 1	[7:6] – 00b = Unspecified Event Data 2 [5:4] – 00b = Unspecified Event Data 3 [3:0] – Event Trigger Offset 1h = State Asserted
15	Event Data 2	Not used
16	Event Data 3	Not used

4.4.3.1 Node Auto Shutdown Sensor – Next Steps

This event is accompanied by specific power supply errors (AC lost, PSU failure, and so on) or other system events. Troubleshoot these events accordingly.

4.5 Power Supply

The BMC monitors the power supply subsystem.

4.5.1 Power Supply Status Sensors

These sensors report the status of the power supplies in the system. When a system first has AC applied or removed, it can log an event. Also, if there is a failure, predictive failure, or a configuration error, it can log an event.

Table 29. Power supply status sensors typical characteristics

Byte	Field	Description
11	Sensor Type	08h = Power Supply
12	Sensor Number	50h = Power Supply 1 Status 51h = Power Supply 2 Status
13	Event Direction and Event Type	[7] Event direction 0b = Assertion Event 1b = Deassertion Event [6:0] Event Type = 6Fh (Sensor Specific)
14	Event Data 1	[7:6] – ED2 data in Table 30 [5:4] – ED3 data in Table 30 [3:0] – Sensor Specific offset as described in Table 30
15	Event Data 2	As described in Table 30
16	Event Data 3	As described in Table 30

Table 30. Power supply status sensor – sensor specific offsets – next steps

Sensor Specific Offset		Description	ED2	ED3	Next Steps
00h	Presence	Power supply detected.	00b = Unspecified Event Data 2	00b = Unspecified Event Data 3	Informational Event
01h	Failure	Power supply failed. Check the data in ED2 and ED3 for more details.	10b = OEM code in Event Data 2 • 01h – Output voltage fault • 02h – Output power fault • 03h – Output overcurrent fault • 04h – Over-temperature fault • 05h – Fan fault	10b = OEM code in Event Data 3 Has the contents of the associated PMBus Status register. For example, Data 3 will have the contents of the VOLTAGE_STATUS register at the time an Output Voltage fault was detected. Refer to the *PMBus Specification* for details on specific register contents.	Indicates that a power supply failed. 1. Remove and reapply AC. 2. If the power supply still fails, replace it.

Sensor Specific Offset		Description	ED2	ED3	Next Steps
02h	Predictive Failure	Check the data in ED2 and ED3 for more details.	10b = OEM code in Event Data 2 • 01h – Output voltage warning • 02h – Output power warning • 03h – Output overcurrent warning • 04h –Over-temperature warning • 05h – Fan warning • 06h – Input under-voltage warning • 07h – Input overcurrent warning • 08h – Input over-power warning	10b = OEM code in Event Data 3 Has the contents of the associated PMBus Status register. For example, Data 3 will have the contents of the VOLTAGE_STATUS register at the time an Output Voltage warning was detected. Refer to the *PMBus Specification* for details on specific register contents.	Depends on the warning event. 1. Replace the power supply. 2. Verify proper airflow to the system. 3. Verify the power source. 4. Replace the system boards.
03h	AC lost	AC removed.	00b = Unspecified Event Data 2	00b = Unspecified Event Data 3	Informational Event.
06h	Configuration error	Power supply configuration is not supported. Check the data in ED2 for more details.	10b = OEM code in Event Data 2 • 01h – The BMC cannot access the PMBus device on the PSU but its FRU device is responding. • 02h – The PMBUS_REVISION command returns a version number that is not supported (only version 1.1 and 1.2 are supported). • 03h – The PMBus device does not successfully respond to the PMBUS_REVISION command. • 04h – The PSU is incompatible with one or more PSUs that are present in the system. • 05h –The PSU FW is operating in a degraded mode (likely due to a failed firmware update).	00b = Unspecified Event Data 3	Indicates that at least one of the supplies is not correct for your system configuration. 1. Remove the power supply and verify compatibility. 2. If the power supply is compatible, it may be faulty. Replace it.

4.5.2 Power Supply Power in Sensors

These sensors log an event when a power supply in the system is exceeding its AC power in threshold.

Table 31. Power supply power in sensors typical characteristics

Byte	Field	Description
11	Sensor Type	0Bh = Other Units
12	Sensor Number	54h = Power Supply 1 Status 55h = Power Supply 2 Status
13	Event Direction and Event Type	[7] Event direction 0b = Assertion Event 1b = Deassertion Event [6:0] Event Type = 01h (Threshold)
14	Event Data 1	[7:6] – 01b = Trigger reading in Event Data 2 [5:4] – 01b = Trigger threshold in Event Data 3 [3:0] – Event Trigger Offset as described in Table 32

Byte	Field	Description
15	Event Data 2	Reading that triggered event
16	Event Data 3	Threshold value that triggered event

The following table describes the severity of each of the event triggers for both assertion and deassertion.

Table 32. Power supply power in sensor – event trigger offset – next steps

Event Trigger Offset		Assertion Severity	Deassertion Severity	Description	Next Steps
07h	Upper non-critical going high	Degraded	OK	PMBus feature to monitor power supply power consumption.	If you see this event, the system is pulling too much power on the input for the PSU rating. 1. Verify the power budget is within the specified range. 2. Check http://www.intel.com/p/en_US/support/ for the power budget tool for your system.
09h	Upper critical going high	Non-fatal	Degraded		

4.5.3 Power Supply Current Out % Sensors

PMBus-compliant power supplies may monitor the current output of the main 12 V voltage rail and report the current usage as a percentage of the maximum power output for that rail.

Table 33. Power supply current out % sensors typical characteristics

Byte	Field	Description
11	Sensor Type	03h = Current
12	Sensor Number	58h = Power Supply 1 Current Out % 59h = Power Supply 2 Current Out %
13	Event Direction and Event Type	[7] Event direction 0b = Assertion Event 1b = Deassertion Event [6:0] Event Type = 01h (Threshold)
14	Event Data 1	[7:6] – 01b = Trigger reading in Event Data 2 [5:4] – 01b = Trigger threshold in Event Data 3 [3:0] – Event Trigger Offset as described in Table 34
15	Event Data 2	Reading that triggered event
16	Event Data 3	Threshold value that triggered event

The following table describes the severity of each of the event triggers for both assertion and deassertion.

Table 34. Power supply current out % sensor – event trigger offset – next steps

Event Trigger Offset		Assertion Severity	Deassertion Severity	Description	Next Steps
07h	Upper non-critical going high	Degraded	OK	PMBus feature to monitor power supply power consumption.	If you see this event, the system is using too much power on the output for the PSU rating. 1. Verify the power budget is within the specified range. 2. Check http://www.intel.com/p/en_US/support/ for the power budget tool for your system.
09h	Upper critical going high	Non-fatal	Degraded		

4.5.4 Power Supply Temperature Sensors

The BMC monitors one or two power supply temperature sensors for each installed PMBus-compliant power supply.

Table 35. Power supply temperature sensors typical characteristics

Byte	Field	Description
11	Sensor Type	01h = Temperature
12	Sensor Number	5Ch = Power Supply 1 Temperature 5Dh = Power Supply 2 Temperature
13	Event Direction and Event Type	[7] Event direction 0b = Assertion Event 1b = Deassertion Event [6:0] Event Type = 01h (Threshold)
14	Event Data 1	[7:6] – 01b = Trigger reading in Event Data 2 [5:4] – 01b = Trigger threshold in Event Data 3 [3:0] – Event Trigger Offset as described in Table 36
15	Event Data 2	Reading that triggered event
16	Event Data 3	Threshold value that triggered event

The following table describes the severity of each of the event triggers for both assertion and deassertion.

Table 36. Power supply temperature sensor – event trigger offset – next steps

Event Trigger Offset		Assertion Severity	Deassertion Severity	Description	Next Steps
07h	Upper non-critical going high	Degraded	OK	An upper non-critical or critical temperature threshold has been crossed.	Check for clear and unobstructed airflow into and out of the chassis. 1. Ensure the SDR is programmed and correct chassis has been selected. 2. Ensure that there are no fan failures. 3. Ensure the air used to cool the system is within the thermal specifications for the system (typically below 35°C).
09h	Upper critical going high	Non-fatal	Degraded		

4.5.5 Power Supply Fan Tachometer Sensors

The BMC polls each installed power supply using the PMBus fan status commands to check for failure conditions for the power supply fans.

Table 37. Power supply fan tachometer sensors typical characteristics

Byte	Field	Description
11	Sensor Type	04h = Fan
12	Sensor Number	A0h = Power Supply 1 Fan Tachometer 1 A1h = Power Supply 1 Fan Tachometer 2 A4h = Power Supply 2 Fan Tachometer 1 A5h = Power Supply 2 Fan Tachometer 2
13	Event Direction and Event Type	[7] Event direction 0b = Assertion Event 1b = Deassertion Event [6:0] Event Type = 03h (“digital” Discrete)
14	Event Data 1	[7:6] – 00b = Unspecified Event Data 2 [5:4] – 00b = Unspecified Event Data 3 [3:0] – Event Trigger Offset = 1h = State Asserted
15	Event Data 2	Not used
16	Event Data 3	Not used

4.5.5.1 Power Supply Fan Tachometer Sensors – Next Steps

These events only get generated in systems with PMBus-capable power supplies and, normally, when the airflow is obstructed to the power supply:

1. Remove and then reinstall the power supply to see whether something might have temporarily caused the fan failure.
2. Swap the power supply with another one to see whether the problem stays with the location or follows the power supply.
3. Replace the power supply depending on the outcome of steps 1 and 2.
4. Ensure the latest FRUSDR update has been run and the correct chassis is detected or selected.

5. Cooling Subsystem

5.1 Fan Sensors

There are three types of fan sensors that can be present on Intel® Server Systems: speed, presence, and redundancy. The last two are only present in systems with hot-swap redundant fans.

5.1.1 Fan Tachometer Sensors

Fan tachometer sensors monitor the rpm signal on the relevant fan headers on the platform. Fan speed sensors are threshold-based sensors. Usually, they only have lower (critical) thresholds set, so that an SEL entry is only generated if the fan spins too slowly.

Table 38. Fan tachometer sensors typical characteristics

Byte	Field	Description
11	Sensor Type	04h = Fan
12	Sensor Number	30h-3Fh (Chassis specific) BAh-BFh (Chassis specific)
13	Event Direction and Event Type	[7] Event direction 0b = Assertion Event 1b = Deassertion Event [6:0] Event Type = 01h (Threshold)
14	Event Data 1	[7:6] – 01b = Trigger reading in Event Data 2 [5:4] – 01b = Trigger threshold in Event Data 3 [3:0] – Event Trigger Offset as described in Table 39
15	Event Data 2	Reading that triggered event
16	Event Data 3	Threshold value that triggered event

The following table describes the severity of each of the event triggers for both assertion and deassertion.

Table 39. Fan tachometer sensor – event trigger offset – next steps

Event Trigger Offset		Assertion Severity	Deassertion Severity	Description	Next Steps
00h	Lower non-critical going low	Degraded	OK	The fan speed has dropped below its lower non-critical threshold.	A fan speed error on a new system build is typically not caused by the fan spinning too slowly; instead, it is caused by the fan being connected to the wrong header (the BMC expects them on certain headers for each chassis and logs this event if there is no fan on that header). 1. Refer to the Quick Start Guide or the Service Guide to identify the correct fan headers to use. 2. Ensure the latest FRUSDR update has been run and the correct chassis is detected or selected. 3. If this was done already, the event may be a sign of impending fan failure (although this only normally applies if the system has been in use for a while). Replace the fan.
02h	Lower critical going low	non-fatal	Degraded	The fan speed has dropped below its lower critical threshold.	

5.1.2 Fan Presence and Redundancy Sensors

Fan presence sensors are only implemented for hot-swap fans, and require an additional pin on the fan header. Fan redundancy is an aggregate of the fan presence sensors and warns when redundancy is lost. Typically, the redundancy mode on Intel Server Systems is an n+1 redundancy (meaning, if one fan fails, there are still sufficient fans to cool the system, but it is no longer redundant) although other modes are also possible.

Table 40. Fan presence sensors typical characteristics

Byte	Field	Description
11	Sensor Type	04h = Fan
12	Sensor Number	40h-4Fh (Chassis specific)
13	Event Direction and Event Type	[7] Event direction 0b = Assertion Event 1b = Deassertion Event [6:0] Event Type = 08h (Generic “digital” Discrete)
14	Event Data 1	[7:6] – 00b = Unspecified Event Data 2 [5:4] – 00b = Unspecified Event Data 3 [3:0] – Event Trigger Offset as described in Table 41
15	Event Data 2	Not used
16	Event Data 3	Not used

The following table describes the severity of each of the event triggers for both assertion and deassertion.

Table 41. Fan presence sensors – event trigger offset – next steps

Event Trigger Offset		Assertion Severity	Deassertion Severity	Description	Next Steps
01h	Device Present	OK	Degraded	Assertion – A fan was inserted. This event may also get logged when the BMC initializes when AC is applied.	Informational only.
				Deassertion – A fan was removed, or was not present at the expected location when the BMC initialized.	These events only get generated in the systems with hot-swappable fans, and normally only when a fan is physically inserted or removed. If fans were not physically removed: 1. Use the Quick Start Guide to check whether the right fan headers were used. 2. Swap the fans round to see whether the problem stays with the location or follows the fan. 3. Replace the fan or fan wiring/housing depending on the outcome of step 2. 4. Ensure the latest FRUSDR update has been run and the correct chassis is detected or selected.

Table 42. Fan redundancy sensors typical characteristics

Byte	Field	Description
11	Sensor Type	04h = Fan
12	Sensor Number	0Ch
13	Event Direction and Event Type	[7] Event direction 0b = Assertion Event 1b = Deassertion Event [6:0] Event Type = 0Bh (Generic Discrete)
14	Event Data 1	[7:6] – 00b = Unspecified Event Data 2 [5:4] – 00b = Unspecified Event Data 3 [3:0] – Event Trigger Offset as described in Table 43
15	Event Data 2	Not used
16	Event Data 3	Not used

The following table describes the severity of each of the event triggers for both assertion and deassertion.

Table 43. Fan redundancy sensor – event trigger offset – next steps

Event Trigger Offset		Description	Next Steps
00h	Fully redundant	The system has lost one or more fans and is running in non-redundant mode. There are enough fans to keep the system properly cooled, but fan speeds will boost.	Fan redundancy loss indicates failure of one or more fans. Look for lower (non-) critical fan errors, or fan removal errors in the SEL, to indicate which fan is causing the problem, and follow the troubleshooting steps for these event types.
01h	Redundancy lost		
02h	Redundancy degraded		
03h	Non-redundant, sufficient from redundant		
04h	Non-redundant, sufficient from insufficient		
05h	Non-redundant, insufficient	The system has lost fans and may no longer be able to cool itself adequately. Overheating may occur if this situation remains for a longer period of time.	
06h	Non-redundant, degraded from fully redundant	The system has lost one or more fans and is running in non-redundant mode. There are enough fans to keep the system properly cooled, but fan speeds will boost.	
07h	Redundant, degraded from non-redundant	The system has lost one or more fans and is running in a degraded mode, but still is redundant. There are enough fans to keep the system properly cooled.	

5.2 Temperature Sensors

There are a variety of temperature sensors that can be implemented on Intel® Server Systems. They are split into various types each with their own events that can be logged.

- Threshold-based Temperature
- Thermal Margin
- Processor Thermal Control %
- Processor DTS Thermal Margin (Monitor only)
- Discrete Thermal
- DIMM Thermal Trip

5.2.1 Threshold-based Temperature Sensors

Threshold-based temperature sensors are sensors that report an actual temperature. These are linear, threshold-based sensors. In most Intel Server Systems, multiple sensors are defined: front panel temperature and baseboard temperature. There are also multiple other sensors that can be defined and are platform-specific. Most of these sensors typically have upper and lower thresholds set – upper to warn in case of an over-temperature situation and lower to warn against sensor failure (temperature sensors typically read out 0 if they stop working).

Table 44. Temperature sensors typical characteristics

Byte	Field	Description
11	Sensor Type	01h = Temperature
12	Sensor Number	See Table 46
13	Event Direction and Event Type	[7] Event direction 0b = Assertion Event 1b = Deassertion Event [6:0] Event Type = 01h (Threshold)
14	Event Data 1	[7:6] – 01b = Trigger reading in Event Data 2 [5:4] – 01b = Trigger threshold in Event Data 3 [3:0] – Event Trigger Offset as described in Table 45
15	Event Data 2	Reading that triggered event
16	Event Data 3	Threshold value that triggered event

Table 45. Temperature sensors event triggers

Event Trigger		Assertion Severity	Deassertion Severity	Description
00h	Lower non-critical going low	Degraded	OK	The temperature has dropped below its lower non-critical threshold.
02h	Lower critical going low	Non-fatal	Degraded	The temperature has dropped below its lower critical threshold.
07h	Upper non-critical going high	Degraded	OK	The temperature has gone over its upper non-critical threshold.
09h	Upper critical going high	Non-fatal	Degraded	The temperature has gone over its upper critical threshold.

Table 46. Temperature sensors – next steps

Sensor #	Sensor Name	Next Steps
21h	Front Panel Temp	If the front panel temperature reads zero, check: • It is connected properly. • The SDR has been programmed correctly for the chassis. If the front panel temperature is too high: • Check the cooling of your server room.
14h	Baseboard Temperature 5	Check for clear and unobstructed airflow into and out of the chassis. • Ensure the SDR is programmed and that the correct chassis has been selected. • Ensure that there are no fan failures. • Ensure the air used to cool the system is within the thermal specifications for the system (typically below 35°C).
15h	Baseboard Temperature 6	
16h	I/O Mod2 Temp	
17h	PCI Riser 5 Temp	
18h	PCI Riser 4 Temp	
20h	Baseboard Temperature 1	
22h	SSB Temperature	
23h	Baseboard Temperature 2	
24h	Baseboard Temperature 3	
25h	Baseboard Temperature 4	
26h	I/O Mod Temp	
27h	PCI Riser 1 Temp	
28h	IO Riser Temp	
2Ch	PCI Riser 2 Temp	
2Dh	SAS Mod Temp	
2Eh	Exit Air Temp	
2Fh	LAN NIC Temp	
D5h	Baseboard Temperature 7	
D6h	Baseboard Temperature 8	

5.2.2 Thermal Margin Sensors

Margin sensors are also linear sensors but typically report a negative value. This is not an actual temperature, but in fact an offset to a critical temperature. Values reported are seen as number of degrees below a critical temperature for the particular component.

The BMC supports DIMM aggregate temperature margin IPMI sensors. The temperature readings from the physical temperature sensors on each DIMM, such as temperature sensor on DIMM (TSOD), are aggregated into IPMI temperature margin sensors for groupings of DIMM slots, the partitioning of which is platform/SKU specific and generally corresponding to fan domains.

The BMC supports global aggregate temperature margin IPMI sensors. There may be as many unique global aggregate sensors as there are fan domains. Each sensor aggregates the readings of multiple other IPMI temperature sensors supported by the BMC firmware. The mapping of child-sensors into each global aggregate sensor is SDR-configurable. The primary usage for these sensors is to trigger turning off fans when a lower threshold is reached.

Table 47. Thermal margin sensors typical characteristics

Byte	Field	Description
11	Sensor Type	01h = Temperature
12	Sensor Number	See Table 49
13	Event Direction and Event Type	[7] Event direction 0b = Assertion Event 1b = Deassertion Event [6:0] Event Type = 01h (Threshold)
14	Event Data 1	[7:6] – 01b = Trigger reading in Event Data 2 [5:4] – 01b = Trigger threshold in Event Data 3 [3:0] – Event Triggers as described in Table 48
15	Event Data 2	Reading that triggered event
16	Event Data 3	Threshold value that triggered event

Table 48. Thermal margin sensors event triggers

Event Trigger		Assertion Severity	Deassertion Severity	Description
07h	Upper non-critical going high	Degraded	OK	The thermal margin has gone over its upper non-critical threshold.
09h	Upper critical going high	non-fatal	Degraded	The thermal margin has gone over its upper critical threshold.

Table 49. Thermal margin sensors – next steps

Sensor #	Sensor Name	Next Steps
74h	P1 Therm Margin	Not a logged SEL event. Sensor is used for thermal management of the processor.
75h	P2 Therm Margin	
76h	P3 Therm Margin	
77h	P4 Therm Margin	
B0h	P1 DIMM Thrm Mrgn1	1. Check for clear and unobstructed airflow into and out of the chassis. 2. Ensure the SDR is programmed and that the correct chassis has been selected. 3. Ensure that there are no fan failures. 4. Ensure the air used to cool the system is within the thermal specifications for the system (typically below 35°C).
B1h	P1 DIMM Thrm Mrgn2	
B2h	P2 DIMM Thrm Mrgn1	
B3h	P2 DIMM Thrm Mrgn2	
B4h	P3 DIMM Thrm Mrgn1	
B5h	P3 DIMM Thrm Mrgn2	
B6h	P4 DIMM Thrm Mrgn1	
B7h	P4 DIMM Thrm Mrgn2	
C8h	Agg Therm Mrgn 1	
C9h	Agg Therm Mrgn 2	
CAh	Agg Therm Mrgn 3	
CBh	Agg Therm Mrgn 4	
CCh	Agg Therm Mrgn 5	
CDh	Agg Therm Mrgn 6	
CEh	Agg Therm Mrgn 7	
CFh	Agg Therm Mrgn 8	

5.2.3 Processor Thermal Control Sensors

The BMC firmware monitors the percentage of time that a processor has been operationally constrained over a given time window (nominally six seconds) due to internal thermal management algorithms engaging to reduce the temperature of the device. This monitoring is instantiated as one IPMI analog/threshold sensor per processor package.

If this is not addressed, the processor will overheat and shut down the system to protect itself from damage.

Table 50. Processor thermal control sensors typical characteristics

Byte	Field	Description
11	Sensor Type	01h = Temperature
12	Sensor Number	78h = Processor 1 Thermal Control % 79h = Processor 2 Thermal Control % 7Ah = Processor 3 Thermal Control % 7Bh = Processor 4 Thermal Control %
13	Event Direction and Event Type	[7] Event direction 0b = Assertion Event 1b = Deassertion Event [6:0] Event Type = 01h (Threshold)
14	Event Data 1	[7:6] – 01b = Trigger reading in Event Data 2 [5:4] – 01b = Trigger threshold in Event Data 3 [3:0] – Event Triggers as described in Table 51
15	Event Data 2	Reading that triggered event
16	Event Data 3	Threshold value that triggered event

Table 51. Processor thermal control sensors event triggers

Event Trigger		Assertion Severity	Deassertion Severity	Description
07h	Upper non-critical going high	Degraded	OK	The thermal margin has gone over its upper non-critical threshold.
09h	Upper critical going high	Non-fatal	Degraded	The thermal margin has gone over its upper critical threshold.

5.2.3.1 Processor Thermal Control % Sensors – Next Steps

These events normally occur due to failures of the thermal solution:

1. Verify heat sink is properly attached and has thermal grease.
2. If the system has a heat sink fan, ensure the fan is spinning.
3. Check all system fans are operating properly.
4. Check that the air used to cool the system is within limits (typically 35 °C).

5.2.4 Processor DTS Thermal Margin Sensors

From Intel® Xeon® processor E5-4600/2600/2400/1600 v2 product families on, there are incorporating a DTS-based thermal spec. This allows a much more accurate control of the thermal solution and enables lower fan speeds and lower fan power consumption. This requires significant BMC firmware calculations to derive the sensor value. BMC's derivation of this value is greatly simplified because the majority of the calculations are performed within the processor itself.

The main usage of this sensor is as an input to the BMC's fan control algorithms. The BMC implements this as a threshold sensor. There is one DTS sensor for each installed physical processor package. Thresholds are not set and alert generation is not enabled for these sensors.

Table 52. Processor DTS thermal margin sensors typical characteristics

Byte	Field	Description
11	Sensor Type	01h = Temperature
12	Sensor Number	83h = Processor 1 DTS Thermal Margin 84h = Processor 2 DTS Thermal Margin 85h = Processor 3 DTS Thermal Margin 86h = Processor 4 DTS Thermal Margin
13	Event Direction and Event Type	[7] Event direction 0b = Assertion Event 1b = Deassertion Event [6:0] Event Type = 01h (Threshold)

5.2.5 Discrete Thermal Sensors

Discrete thermal sensors do not report a temperature at all; instead, they report an overheating event of some kind. For example, VRD Hot (voltage regulator is overheating) or processor Thermal Trip (the processor got so hot that its over-temperature protection was triggered and the system was shut down to prevent damage).

5.2.5.1 SSB Thermal Trip Sensor

Table 53. SSB thermal trip sensors typical characteristics

Byte	Field	Description
11	Sensor Type	01h = Temperature
12	Sensor Number	0Dh = SSB Thermal Trip
13	Event Direction and Event Type	[7] Event direction 0b = Assertion Event 1b = Deassertion Event [6:0] Event Type = 03h (Digital Discrete)
14	Event Data 1	[7:6] – 00b = Unspecified Event Data 2 [5:4] – 00b = Unspecified Event Data 3 [3:0] – Event Trigger Offset = 01h (State Asserted, South Side Bridge (SSB) overheated)
15	Event Data 2	Not used
16	Event Data 3	Not used

5.2.5.2 VRD HOT Sensor

Table 54. VRD HOT sensor typical characteristics

Byte	Field	Description
11	Sensor Type	01h = Temperature
12	Sensor Number	90h = SSB Thermal Trip
13	Event Direction and Event Type	[7] Event direction 0b = Assertion Event 1b = Deassertion Event [6:0] Event Type = 05h (Digital Discrete)
14	Event Data 1	[7:6] – 10b = OEM code in Event Data 2 [5:4] – 10b = OEM code in Event Data 3 [3:0] – Event Trigger Offset = 01h (Limit Exceeded)
15	Event Data 2	Processor VRD HOT bitmap [7:4] - Reserved [3] - CPU4 [2] - CPU3 [1] - CPU2 [0] – CPU1
16	Event Data 3	Memory VRD HOT bitmap [7] – CPU4, DIMM Channel3/4 [6] – CPU4, DIMM Channel1/2 [5] – CPU3, DIMM Channel3/4 [4] – CPU3, DIMM Channel1/2 [3] – CPU2, DIMM Channel3/4 [2] – CPU2, DIMM Channel1/2 [1] – CPU1, DIMM Channel3/4 [0] – CPU1, DIMM Channel1/2

5.2.5.3 Discrete Thermal Sensors – Next Steps

1. Check for clear and unobstructed airflow into and out of the chassis.
2. Ensure the SDR is programmed and that the correct chassis has been selected.
3. Ensure that there are no fan failures.
4. Ensure the air used for cooling the system is within the thermal specifications for the system (typically below 35 °C).

5.2.6 DIMM Thermal Trip Sensors

The BMC supports DIMM Thermal Trip monitoring that is instantiated as one aggregate IPMI discrete sensor per processor. When a DIMM Thermal Trip occurs, the system hardware automatically powers down the server and the BMC asserts the sensor offset and logs an event.

Table 55. DIMM thermal trip typical characteristics

Byte	Field	Description
11	Sensor Type	0Ch = Memory
12	Sensor Number	C0h = Processor 1 DIMM Thermal Trip C1h = Processor 2 DIMM Thermal Trip C2h = Processor 3 DIMM Thermal Trip C3h = Processor 4 DIMM Thermal Trip
13	Event Direction and Event Type	[7] Event direction 0b = Assertion Event 1b = Deassertion Event [6:0] Event Type = 6Fh (Sensor Specific)
14	Event Data 1	[7:6] – 00b = Unspecified Event Data 2 [5:4] – 10b = OEM code in Event Data 3 [3:0] – Event Trigger Offset = 0A = Critical over temperature
15	Event Data 2	Not used
16	Event Data 3	[7:5] – Socket ID 0–3 = CPU1-4 [4:3] – Channel 0–3 = Channel A, B, C, D for CPU1 Channel E, F, G, H for CPU2 Channel J, K, L, M for CPU3 Channel N, P, R, T for CPU4 [2:0] – DIMM 0–2 = DIMM 1–3 on Channel

5.2.6.1 DIMM Thermal Trip Sensors – Next Steps

1. Check for clear and unobstructed airflow into and out of the chassis.
2. Ensure the SDR is programmed and that the correct chassis has been selected.
3. Ensure that there are no fan failures.
4. Ensure the air used to cool the system is within the thermal specifications for the system (typically below 35 °C).

5.2.7 NVMe* Thermal Status

The BMC supports NVMe temperature and critical warning monitoring that is instantiated as one aggregate IPMI discrete sensor per HSBP. Each backplane provides a single temperature sensor. The aggregate sensor reports the temperature of the hottest drive inserted into the HSBP. The BMC uses the NVMe drive's SMBus Management Interface (I^2C address 0xD4 byte 3) to retrieve temperature data. Because discrete temperature sensors were deprecated early in the NVMe drive life-cycle, drive temperature is never acquired from a discrete sensor on the drive. The BMC, as a result, can only rely on temperature data acquired via the Management Interface.

The features described here require specific pieces of hardware, and are enabled by sensor data records. To be eligible, a system must have the following properties:

- Intel® Server Board S2600WF family, Intel® Server Board S2600BP family, or Intel® Server Board S2600ST family.
- NVMe*-capable HSBP.
- Intel® Server Board S2600WF family and Intel® Server Board S2600ST family require OCuLink cables. One is required for each slot that holds an NVMe drive. The I^2C ASIC on the drive fails to operate without the OCuLink cable.
- Intel® SSD DC P3700 series (or later) NVMe SSD with firmware revision level MR5 (or later).

5.2.7.1 NVMe* Temperature Sensor

The NVMe temperature SEL occurs when the aggregate temperature sensor reading reaches the upper critical threshold. In order to report which of several drives are over temp, OEM Extended data bytes are used. The remainder of the SEL uses standard temperature sensor decoding rules. The NVMe Temperature SEL uses a new format for the OEM Extended data bytes.

Table 56. NVMe* temperature sensor typical characteristics

Byte	Field	Description
11	Sensor Type	01h = Temperature
12	Sensor Number	91h = NVMe 1 Therm Mgn 92h = NVMe 2 Therm Mgn 93h = NVMe 3 Therm Mgn
13	Event Direction and Event Type	[7] Event direction 0b = Assertion Event 1b = Deassertion Event [6:0] Event Type = 01h (Threshold)
14	Event Data 1	[7:6] – 10b = Trigger reading in Event Data 2 [5:4] – 10b = Trigger threshold in Event Data 3 [3:0] – 0001b = OEM Event Trigger in Table 45
15	Event Data 2	Reading that triggered event
16	Event Data 3	Threshold value that triggered event
17	Extended Data 1	[7] = Extended format indicator [6:4] = # Extended Data byte [3:2] = reserved [1:0] = Existing severity encoding
18	Extended Data 2	0 = Reserved 1 = Drive Position Format 2 = Critical Warning Format 3 = Add-in card format 4-0xff = Reserved
19	Extended Data 3	For Format = 1 (Drive Position Format), ExtData[2] is a bitfield indicating which drives are over temperature. Bit 0 set indicates Drive 0 is over temp. Bit 7 set indicates Drive 7 is over temp.
20	Extended Data 4	If Extended Data 1 indicate this byte is included, same format with above byte.
21	Extended Data 5	If Extended Data 1 indicate this byte is included, same format with above byte.
22	Extended Data 6	If Extended Data 1 indicate this byte is included, same format with above byte.
23	Extended Data 7	If Extended Data 1 indicate this byte is included, same format with above byte.
24	Extended Data 8	If Extended Data 1 indicate this byte is included, same format with above byte.

5.2.7.2 NVMe* Critical Warning Sensor

The critical warning sensor aggregates a set of SMART drive warning flags. For the first warning bit asserted for a drive, a corresponding critical warning SEL is generated.

Table 57. NVMe* critical warning sensor typical characteristics

Byte	Field	Description
11	Sensor Type	0Dh=Disk drive
12	Sensor Number	94h = NVMe* 1 Crit Warn 95h = NVMe 2 Crit Warn 96h = NVMe 3 Crit Warn
13	Event Direction and Event Type	[7] Event direction 0b = Assertion Event 1b = Deassertion Event [6:0] Event Type = 73h (OEM Discrete)
14	Event Data 1	0x8x (low nibble is the drive causing the event, zero based count)
15	Event Data 2	SMART warning byte defined in Table 58 for the drive number indicated by the low nibble of ED1.
16	Event Data 3	Not used

Table 58. SMART warning bits

Bit	Assertion value	Message
0	1	Spare space below threshold
1	1	Temperature above or below threshold
2	1	NVMe* reliability degraded
3	1	In read-only mode
4	1	Volatile backup service failed
5–7	X	Reserved

5.3 System Airflow Monitoring Sensor

The BMC provides an IPMI sensor to report the volumetric system airflow in cubic feet per minute (CFM). The airflow in CFM is calculated based on the system fan pulse width modulation (PWM) values. The specific PWM used to determine the CFM is SDR-configurable. The relationship between PWM and CFM is based on a lookup table in an OEM SDR.

The airflow data is used in the calculation for exit air temperature monitoring. It is exposed as an IPMI sensor to allow a data center management application to access this data for use in rack-level thermal management.

This sensor is informational only and does not log events into the SEL.

6. Processor Subsystem

Intel® Server Systems report multiple processor-centric sensors in the SEL.

6.1 Processor Status Sensor

The BMC provides an IPMI sensor of type processor for monitoring status information for each processor slot. If an event state (sensor offset) has been asserted, it remains asserted until one of the following happens:

- A rearm Sensor Events command is executed for the processor status sensor.
- AC or DC power cycle, system reset, or system boot occurs.

CPU Presence status is not saved across AC power cycles and therefore does not generate a deassertion after cycling AC power.

Table 59. Process status sensors typical characteristics

Byte	Field	Description
11	Sensor Type	07h = Processor
12	Sensor Number	70h = Processor 1 Status 71h = Processor 2 Status 72h = Processor 3 Status 73h = Processor 4 Status
13	Event Direction and Event Type	[7] Event direction 0b = Assertion Event 1b = Deassertion Event [6:0] Event Type = 6Fh (Sensor Specific)
14	Event Data 1	[7:6] – 00b = Unspecified Event Data 2 10b = OEM code in Byte2 [5:4] – 00b = Unspecified Event Data 3 [3:0] – Event Trigger Offset as described in Table 60
15	Event Data 2	For Thermal Trip event type: 0x00 – CPU non-recoverable over-temp condition 0x01 – CPU boot FIVR fault For other event: Not used
16	Event Data 3	Not used

Table 60. Processor status sensors – next steps

Event Trigger Offset	Processor Status	Next Steps
0h	Internal error (IERR)	1. Cross test the processors. 2. Replace the processors depending on the results of the test.
1h	Thermal trip	This event normally only happens due to failures of the thermal solution: 1. Verify that heat sink is properly attached and has thermal grease. 2. If the system has a heat sink fan, ensure the fan is spinning. 3. Check that all system fans are operating properly. 4. Check that the air used to cool the system is within limits (typically 35 °C).
2h	FRB1/BIST failure	1. Cross test the processors. 2. Replace the processors depending on the results of the test.
3h	FRB2/Hang in POST failure	
4h	FRB3/Processor startup/initialization failure (CPU fails to start)	
5h	Configuration error (for DMI)	
6h	SM BIOS uncorrectable CPU-complex error	
7h	Processor presence detected	Informational Event
8h	Processor disabled	1. Cross test the processors. 2. Replace the processors depending on the results of the test.
9h	Terminator presence detected	

6.2 Internal Error Sensor

When the Catastrophic Error signal (CATERR#) stays asserted, it is a sign that something serious has gone wrong in the hardware. The BMC monitors this signal and reports when it stays asserted.

Table 61. Internal error sensor typical characteristics

Byte	Field	Description
11	Sensor Type	07h = Processor
12	Sensor Number	80h
13	Event Direction and Event Type	[7] Event direction 0b = Assertion Event 1b = Deassertion Event [6:0] Event Type = 03h (Digital Discrete)
14	Event Data 1	[7:6] – 10b = OEM code in Event Data 2 [5:4] – 10b = OEM code in Event Data 3 [3:0] – Event Trigger Offset = 1h (State Asserted)
15	Event Data 2	Event Data 2 values as described in Table 62.
16	Event Data 3	Bitmap of the CPU that causes the system CATERR. [0]: CPU1 [1]: CPU2 [2]: CPU3 [3]: CPU4 **Note**: If more than one bit is set, the BMC cannot determine the source of the CATERR.

Table 62. Internal error sensor – event data 2 values – next steps

ED2	Description	Next Steps
00h	Unknown	1. Cross test the processors. 2. Replace the processors depending on the results of the test.
01h	CATERR	This error is typically caused by other platform components. 1. Check for other errors near the time of the CATERR event. 2. Verify all peripherals are plugged in and operating correctly, particularly hard drives, optical drives, and I/O. 3. Update system firmware and drivers.
2h	CPU Core Error	1. Cross test the processors. 2. Replace the processors depending on the results of the test.
3h	MSID Mismatch	Verify that the processor is supported by the baseboard. Check the board *Technical Product Specification (TPS).*

6.3 IERR Recovery Dump Info Sensor

If a CATERR-low condition is detected, the BMC tries to dump the corresponding register, which can be used to analyze the reason of IERR. The default action after register dump is to reset the system. The BIOS setup utility provides an option to disable or enable system reset by the BMC for detection of this condition. If any required register cannot be dumped and system reset is enabled, then a reset is done. After the above actions are completed, the BMC tries to notify BIOS to pause and then dump again. If it still failed to dump registers, BMC resets the system after logging this event and POST code to the SEL.

Table 63. Internal error sensor typical characteristics

Byte	Field	Description
11	Sensor Type	D1h = OEM sensor type
12	Sensor Number	7Dh
13	Event Direction and Event Type	[7] Event direction 0b = Assertion Event 1b = Deassertion Event [6:0] Event Type = 70h (OEM)
14	Event Data 1	[7:6] – 10b = OEM code in Event Data 2 [5:4] – 00b = Unspecified Event Data 3 [3:0] – Event Trigger Offset = 1h (Dump Failed)
15	Event Data 2	Bitmap of dump failed register type [7:5] – Reserved [4] - MCA error source register [3] - PCI config space [2] - IIO register [1] - Core MSR registers [0] - Uncore MSR register
16	Event Data 3	0xFF
17	Extension Event Data 1	[7:4] – Number of valid extension bytes following the first one [3:0] - Reserved
18	Extension Event Data 2	[7:0] - POST code

6.3.1 IERR Recovery Dump Info Sensor – Next Steps

1. Check for other errors near the time of the IERR Recovery Dump Info event.
2. Verify all peripherals are plugged in and operating correctly, particularly hard drives, optical drives, and I/O.
3. Update system firmware and drivers.

6.4 CPU Missing Sensor

The CPU Missing sensor is a discrete sensor that only reports if the processor is not installed. The most common instance of this event is due to a processor populated in an incorrect socket.

Table 64. CPU missing sensor typical characteristics

Byte	Field	Description
11	Sensor Type	07h = Processor
12	Sensor Number	82h
13	Event Direction and Event Type	[7] Event direction 0b = Assertion Event 1b = Deassertion Event [6:0] Event Type = 6Fh (Sensor Specific)
14	Event Data 1	[7:6] – 00b = Unspecified Event Data 2 [5:4] – 00b = Unspecified Event Data 3 [3:0] – Event Trigger Offset = 1h (State Asserted)
15	Event Data 2	Not used
16	Event Data 3	Not used

6.4.1 CPU Missing Sensor – Next Steps

Verify the processor is installed in the correct slot.

6.5 Intel® Ultra Path Interconnect (Intel® UPI) Sensors

The Intel® Ultra Path Interconnect (Intel® UPI) bus on Intel® Server Boards based on Intel® Xeon® processor E5-4600/2600/2400/1600/1400 product families is the interconnect between processors.

The Intel® UPI Link Width Reduced sensor is used by the BIOS POST to report when the link width has been reduced. Therefore, the Generator ID is 01h.

The Intel® UPI Error sensors are reported by the BIOS SMI Handler to the BMC, so the Generator ID is 33h.

6.5.1 Intel® Ultra Path Interconnect (Intel® UPI) Link Width Reduced Sensor

BIOS POST has reduced the Intel® UPI Link Width because of an error condition seen during initialization.

Table 65. Intel® Ultra Path Interconnect (Intel® UPI) link width reduced sensor typical characteristics

Byte	Field	Description
8, 9	Generator ID	0001h = BIOS POST
11	Sensor Type	13h = Critical Interrupt
12	Sensor Number	09h
13	Event Direction and Event Type	[7] Event direction 0b = Assertion Event 1b = Deassertion Event [6:0] Event Type = 77h (OEM Discrete)
14	Event Data 1	[7:6] – 10b = OEM code in Event Data 2 [5:4] – 00b = Unspecified Event Data 3 [3:0] – Event Trigger Offset 1h = Reduced to ½ width 2h = Reduced to ¼ width
15	Event Data 2	0–3 = CPU1-4
16	Event Data 3	Not used

6.5.1.1 Intel® Ultra Path Interconnect (Intel® UPI) Link Width Reduced Sensor – Next Steps

If the error continues:

1. Check if the processor is installed correctly.
2. Inspect the socket for bent pins.
3. Cross test the processor. If the issue remains with the processor socket, replace the main board; otherwise replace the processor.

6.5.2 Intel® Ultra Path Interconnect (Intel® UPI) Correctable Error Sensor

The system detected an error and corrected it. This is an informational event.

Table 66. Intel® Ultra Path Interconnect (Intel® UPI) correctable error sensor typical characteristics

Byte	Field	Description
8, 9	Generator ID	0033h = BIOS SMI Handler
11	Sensor Type	13h = Critical Interrupt
12	Sensor Number	06h
13	Event Direction and Event Type	[7] Event direction 0b = Assertion Event 1b = Deassertion Event [6:0] Event Type = 72h (OEM Discrete)
14	Event Data 1	[7:6] – 10b = OEM code in Event Data 2 [5:4] – 00b = Unspecified Event Data 3 [3:0] – Event Trigger Offset = Reserved
15	Event Data 2	0–3 = CPU1-4
16	Event Data 3	Not used

6.5.2.1 Intel® Ultra Path Interconnect (Intel® UPI) Correctable Error Sensor – Next Steps

This is an Informational event only. Correctable errors are acceptable and normal at a low rate of occurrence. If the error continues:

1. Check if the processor is installed correctly.
2. Inspect the socket for bent pins.
3. Cross test the processor. If the issue remains with the processor socket, replace the main board, otherwise the processor.

6.6 Processor ERR2 Timeout Sensor

The BMC supports an ERR2 Timeout Sensor that asserts if any CPU's ERR2 signal has been asserted for longer than a fixed time period (> 90 seconds). ERR[2] is a processor signal that indicates when the IIO (Integrated IO module in the processor) has a fatal error, which could not be communicated to the core to trigger SMI. ERR[2] events are fatal error conditions, where the BIOS and operating system will attempt to gracefully handle error, but may not always do so reliably. A continuously asserted ERR2 signal is an indication that the BIOS cannot service the condition that caused the error. This is usually because that condition prevents the BIOS from running.

When an ERR2 timeout occurs, the BMC asserts/deasserts the ERR2 Timeout Sensor, and logs a SEL event for that sensor. The default behavior for BMC core firmware is to initiate a system reset upon detection of an ERR2 timeout. The BIOS setup utility provides an option to disable or enable system reset by the BMC on detection of this condition.

Table 67. Processor ERR2 timeout sensor typical characteristics

Byte	Field	Description
11	Sensor Type	07h = Processor
12	Sensor Number	7Ch = Processor ERR2 Timeout
13	Event Direction and Event Type	[7] Event direction 0b = Assertion Event 1b = Deassertion Event [6:0] Event Type = 03h (“digital” discrete)
14	Event Data 1	[7:6] – 10b = OEM code in Event Data 2 [5:4] – 00b = Unspecified Event Data 3 [3:0] – Event Trigger Offset = 1h (State Asserted)
15	Event Data 2	[7:4] – Not used [3:0] – Bitmap of the CPU that causes the ERR2 timeout. [0]: CPU1 [1]: CPU2 [2]: CPU3 [3]: CPU4
16	Event Data 3	Not used

6.6.1 Processor ERR2 Timeout – Next Steps

Check the SEL for any other events around the time of the failure.

Take note of all IPMI activity that was occurring around the time of the failure. Capture a System BMC Debug Log as soon as possible after experiencing this failure. This log can be captured from the Integrated BMC Web Console or by using the Intel® Server Configuration Utility (`syscfg/sbmcdl Public filename.zip`). Send the log file to the system manufacturer or Intel representative for failure analysis.

7. Memory Subsystem

Intel® servers report memory errors, status, and configuration in the SEL.

7.1 Memory RAS Configuration Status

A Memory RAS Configuration Status event is logged after an AC power-on occurs, only if any RAS Mode is currently configured, and only if RAS Mode is successfully initiated.

This is to make sure that there is a record in the SEL telling what the RAS Mode was at the time that the system started up. This is only logged after AC power-on, not DC power-on.

The Memory RAS Configuration Status Sensor is also used to log an event during POST whenever there is a RAS configuration error. This is a case where a RAS Mode has been selected but when the system boots, the memory configuration cannot support the RAS Mode. The memory configuration fails, and operates in Independent Channel Mode.

In the SEL record logged, the ED1 Offset value is “RAS Configuration Disabled”, and ED3 contains the RAS Mode that is currently selected but could not be configured. ED2 gives the reason for the RAS configuration failure – at present, only two “RAS Configuration Error Type” values are implemented:

0 = None – This is used for an AC power-on log record when the RAS configuration is successfully configured.

3 = Invalid DIMM Configuration for RAS Mode – The installed DIMM configuration cannot support the currently selected RAS Mode. This may be due to DIMMs that have failed or been disabled, so when this reason has been logged, the user should check the preceding SEL events to see whether there are DIMM error events.

Table 68. Memory RAS configuration status sensor typical characteristics

Byte	Field	Description
8, 9	Generator ID	0001h = BIOS POST
11	Sensor Type	0ch = Memory
12	Sensor Number	02h
13	Event Direction and Event Type	[7] Event direction 0b = Assertion Event 1b = Deassertion Event [6:0] Event Type = 09h (digital Discrete)
14	Event Data 1	[7:6] – 10b = OEM code in Event Data 2 [5:4] – 10b = OEM code in Event Data 3 [3:0] – Event Trigger Offset as described in Table 69
15	Event Data 2	RAS Configuration Error Type [7:4] = Reserved [3:0] = Configuration Error 0 = None 3 = Invalid DIMM Configuration for RAS Mode All other values are reserved.
16	Event Data 3	RAS Mode Configured [7:4] = Reserved [3:0] = RAS Mode 0h = None (Independent Channel Mode) 1h = Mirroring Mode 2h = Lockstep Mode 4h = Rank Sparing Mode

Table 69. Memory RAS configuration status sensor – event trigger offset – next steps

Event Trigger Offset		Description	Next Steps
01h	RAS configuration enabled.	User enabled mirrored channel mode in setup.	Informational event only.
00h	RAS configuration disabled.	Mirrored channel mode is disabled (either in setup or due to unavailability of memory at post, in which case post error 8500 is also logged).	• If this event is accompanied by a post error 8500, there was a problem applying the mirroring configuration to the memory. Check for other errors related to the memory and troubleshoot accordingly. • If there is no post error, mirror mode was simply disabled in BIOS setup and this should be considered informational only.

7.2 Memory RAS Mode Select

Memory RAS Mode Select events are logged to record changes in RAS Mode.

When a RAS Mode selection is made that changes the RAS Mode (including selecting a RAS Mode from or to Independent Channel Mode), that change is logged to SEL in a Memory RAS Mode Select event message, which records the previous RAS Mode (from) and the newly selected RAS Mode (to). The event also includes an Offset value in ED1, which indicates whether the mode change left the system with a RAS Mode active (Enabled), or not (Disabled – Independent Channel Mode selected). This sensor provides the Spare Channel mode RAS Configuration status. Memory RAS Mode Select is an informational event.

Table 70. Memory RAS mode select sensor typical characteristics

Byte	Field	Description
8, 9	Generator ID	0001h = BIOS POST
11	Sensor Type	0ch = Memory
12	Sensor Number	12h
13	Event Direction and Event Type	[7] Event direction 0b = Assertion Event 1b = Deassertion Event [6:0] Event Type = 09h (digital Discrete)
14	Event Data 1	[7:6] – 10b = OEM code in Event Data 2 [5:4] – 10b = OEM code in Event Data 3 [3:0] – Event Trigger Offset 0h = RAS Configuration Disabled 1h = RAS Configuration Enabled
15	Event Data 2	Prior RAS Mode [7:4] = Reserved [3:0] = RAS Mode 0h = None (Independent Channel Mode) 1h = Mirroring Mode 2h = Lockstep Mode 4h = Rank Sparing Mode
16	Event Data 3	Selected RAS Mode [7:4] = Reserved [3:0] = RAS Mode 0h = None (Independent Channel Mode) 1h = Mirroring Mode 2h = Lockstep Mode 4h = Rank Sparing Mode

7.3 Mirroring Redundancy State

Mirroring Mode protects memory data by full redundancy – keeping complete copies of all data on both channels of a Mirroring Domain (channel pair). If an Uncorrectable Error, which is normally fatal, occurs on one channel of a pair, and the other channel is still intact and operational, then the Uncorrectable Error is "demoted" to a Correctable Error, and the failed channel is disabled. Because the Mirror Domain is no longer redundant, a Mirroring Redundancy State SEL Event is logged.

For different platforms, there are some differences in the event definition. For the following product families, refer to Table 71.

- Intel® Server Board based on Intel® Xeon® processor E5-1600/2600/4600 v2 product family
- Intel® Server Board based on Intel® Xeon® processor E5-2400 v2 product family
- Intel® Server Board based on Intel® Xeon® processor E5-2600 v3/v4 product family
- Intel® Server Board based on Intel® Xeon® processor E3-1200 v2/v3/v4 product family
- Intel® Server Board based on Intel® Xeon® processor E3-1200 v5/v6 product family
- Intel® Server Board based on Intel® Xeon Phi™ product family

Table 71. Mirroring redundancy state sensor typical characteristics

Byte	Field	Description
8, 9	Generator ID	0033h = BIOS SMI Handler
11	Sensor Type	0ch = Memory
12	Sensor Number	01h
13	Event Direction and Event Type	[7] Event direction 0b = Assertion Event 1b = Deassertion Event [6:0] Event Type = 0Bh (Generic Discrete)
14	Event Data 1	[7:6] – 10b = OEM code in Event Data 2 [5:4] – 10b = OEM code in Event Data 3 [3:0] – Event Trigger Offset 0h = Fully Redundant 2h = Redundancy Degraded
15	Event Data 2	Location [7:4] = Mirroring Domain 0–1 = Channel Pair for Socket [3:2] = Reserved [1:0] = Rank on DIMM 0–3 = Rank Number
16	Event Data 3	Location [7:5] = Socket ID 0–3 = CPU1-4 [4:3] = Channel 0–3 = Channel A, B, C, D for CPU1 Channel E, F, G, H for CPU2 Channel J, K, L, M for CPU3 Channel N, P, R, T for CPU4 [2:0] = DIMM 0–2 = DIMM 1–3 on Channel

For the following product family, refer to Table 72.

- Intel® Server Board based on Intel® Xeon® Scalable processor family
- Intel® Server Board based on 2nd Gen Intel® Xeon® Scalable processor family
- Intel® Server Board based on Intel® Xeon® Platinum 9200 processor family

Table 72. Mirroring redundancy state sensor typical characteristics for Intel® Server Boards based on Intel® Server Board based on Intel® Xeon® Scalable processor family and Intel® Server Board based on 2nd Gen Intel® Xeon® Scalable processor family

Byte	Field	Description
8, 9	Generator ID	0033h = BIOS SMI Handler
11	Sensor Type	0ch = Memory
12	Sensor Number	01h
13	Event Direction and Event Type	[7] Event direction 0b = Assertion Event 1b = Deassertion Event [6:0] Event Type = 0Bh (Generic Discrete)
14	Event Data 1	[7:6] – 10b = OEM code in Event Data 2 [5:4] – 10b = OEM code in Event Data 3 [3:0] – Event Trigger Offset 0h = Fully Redundant 2h = Redundancy Degraded
15	Event Data 2	Location [7:4] = DIMM index 0-x = DIMM index per Channel [3:0] = Rank index 0-x = Physical rank index per DIMM As described in Table 91
16	Event Data 3	Location [7:4] = Socket index 0–3 = CPU1-4 [3:0] = Channel index 0-x = Channel index for Socket As described in Table 92

7.3.1 Mirroring Redundancy State Sensor – Next Steps

This event is accompanied by memory errors indicating the source of the issue. Troubleshoot accordingly (probably replace affected DIMM).

For boards with DIMM Fault LEDs, the appropriate Fault LED is lit to indicate which DIMM was the source of the error triggering the Mirroring Failover action, that is, the failing DIMM.

7.4 Sparing Redundancy State

Rank Sparing Mode is a Memory RAS configuration option that reserves one memory rank per channel as a “spare rank”. If any rank on a given channel experiences enough Correctable ECC Errors to cross the Correctable Error Threshold, the data in that rank is copied to the spare rank, and then the spare rank is mapped into the memory array to replace the failing rank.

Rank Sparing Mode protects memory data by reserving a “Spare Rank” on each channel that has memory installed on it. If a Correctable Error Threshold event occurs, the data from the failing rank is copied to the Spare Rank on the same channel, and the failing DIMM is disabled. Because the Sparing Domain is no longer redundant, a Sparing Redundancy State SEL Event is logged.

Table 73. Sparing redundancy state sensor typical characteristics

Byte	Field	Description
8, 9	Generator ID	0033h = BIOS SMI Handler
11	Sensor Type	0ch = Memory
12	Sensor Number	11h
13	Event Direction and Event Type	[7] Event direction 0b = Assertion Event 1b = Deassertion Event [6:0] Event Type = 0Bh (Generic Discrete)
14	Event Data 1	[7:6] – 10b = OEM code in Event Data 2 [5:4] – 10b = OEM code in Event Data 3 [3:0] – Event Trigger Offset 0h = Fully Redundant 2h = Redundancy Degraded
15	Event Data 2	Location [7:4] = Sparing Domain 0–3 = Channel A-D for Socket [3:2] = Reserved [1:0] = Rank on DIMM 0–3 = Rank Number
16	Event Data 3	Location [7:5]= Socket ID 0–3 = CPU1-4 [4:3] = Channel 0–3 = Channel A, B, C, D for CPU1 Channel E, F, G, H for CPU2 Channel J, K, L, M for CPU3 Channel N, P, R, T for CPU4 [2:0] = DIMM 0–2 = DIMM 1–3 on Channel

7.4.1 Sparing Redundancy State Sensor – Next Steps

This event is accompanied by memory errors indicating the source of the issue. Troubleshoot accordingly (probably replace affected DIMM).

For boards with DIMM Fault LEDs, the appropriate Fault LED is lit to indicate which DIMM was the source of the error triggering the Mirroring Failover action, that is, the failing DIMM.

7.5 ECC and Address Parity

1. Memory data errors are logged as correctable or uncorrectable.
2. Uncorrectable errors are fatal.
3. Memory addresses are protected with parity bits and a parity error is logged. This is a fatal error.

7.5.1 Memory Correctable and Uncorrectable ECC Error

ECC errors are divided into Uncorrectable ECC Errors and Correctable ECC Errors. A “Correctable ECC Error” actually represents a threshold overflow. More Correctable Errors are detected at the memory controller level for a given DIMM within a given timeframe. In both cases, the error can be narrowed down to particular DIMM(s). The BIOS SMI error handler uses this information to log the data to the BMC SEL and identify the failing DIMM.

For different platforms, there are some differences in the event definition. For the following product families, refer to Table 74.

- Intel® Server Board based on Intel® Xeon® processor E5-1600/2600/4600 v2 product family
- Intel® Server Board based on Intel® Xeon® processor E5-2400 v2 product family
- Intel® Server Board based on Intel® Xeon® processor E5-2600 v3/v4 product family
- Intel® Server Board based on Intel® Xeon® processor E3-1200 v2/v3/v4 product family
- Intel® Server Board based on Intel® Xeon® processor E3-1200 v5/v6 product family

Table 74. Correctable and uncorrectable ECC error sensor typical characteristics

Byte	Field	Description
8, 9	Generator ID	0033h = BIOS SMI Handler
11	Sensor Type	0ch = Memory
12	Sensor Number	02h
13	Event Direction and Event Type	[7] Event direction 0b = Assertion Event 1b = Deassertion Event [6:0] Event Type = 6Fh (Sensor Specific)
14	Event Data 1	[7:6] – 10b = OEM code in Event Data 2 [5:4] – 10b = OEM code in Event Data 3 [3:0] – Event Trigger Offset as described in Table 77
15	Event Data 2	[7:2] – Reserved. Set to 0. [1:0] – Rank on DIMM 0–3 = Rank number
16	Event Data 3	[7:5] – Socket ID 0–3 = CPU1-4 [4:3] –Channel 0–3 = Channel A, B, C, D for CPU1 Channel E, F, G, H for CPU2 Channel J, K, L, M for CPU3 Channel N, P, R, T for CPU4 [2:0] DIMM 0–2 = DIMM 1–3 on Channel

For the following product families, refer to Table 75.

- Intel® Server Board based on Intel® Xeon Phi™ product family
- Intel® Server Board based on Intel® Xeon® Scalable processor family
- Intel® Server Board based on 2nd Gen Intel® Xeon® Scalable processor family

Table 75. Correctable and uncorrectable ECC error sensor typical characteristics for Intel® Server Boards based on Intel® Xeon Phi™ product family, Intel® Server Boards based on Intel® Xeon® Scalable processor family, Intel® Server Board based on 2nd Gen Intel® Xeon® Scalable processor family

Byte	Field	Description
8, 9	Generator ID	0033h = BIOS SMI Handler
11	Sensor Type	0ch = Memory
12	Sensor Number	02h
13	Event Direction and Event Type	[7] Event direction 0b = Assertion Event 1b = Deassertion Event [6:0] Event Type = 6Fh (Sensor Specific)
14	Event Data 1	[7:6] – 10b = OEM code in Event Data 2 [5:4] – 10b = OEM code in Event Data 3 [3:0] – Event Trigger Offset as described in Table 77
15	Event Data 2	[7:4] – DIMM index 0-x = DIMM index per Channel [3:0] – Rank index(Physical rank index per DIMM) As described in Table 91
16	Event Data 3	[7:4] – Socket index 0–3 = CPU1-4 [3:0] – Channel index 0-x = Channel index for Socket As described in Table 92

For the following product families, refer to Table 76.

- Intel® Server Board based on Intel® Xeon® Platinum 9200 processor family

Table 76. Correctable and uncorrectable ECC error sensor typical characteristics for Intel® Server Board based on Intel® Xeon® Platinum 9200 processor family

Byte	Field	Description
8, 9	Generator ID	0033h = BIOS SMI Handler
11	Sensor Type	0ch = Memory
12	Sensor Number	02h
13	Event Direction and Event Type	[7] Event direction 0b = Assertion Event 1b = Deassertion Event [6:0] Event Type = 6Fh (Sensor Specific)
14	Event Data 1	[7:6] – 10b = OEM code in Event Data 2 [5:4] – 10b = OEM code in Event Data 3 [3:0] – Event Trigger Offset as described in Table 77
15	Event Data 2	[7:4]=DIMM Index 0–1=DIMM1-2, DIMM index per Channel [3:0]=Physical rank index per DIMM
16	Event Data 3	[7:4] = Socket index 0=CPU0_0 1=CPU0_1 2=CPU1_0 3=CPU1_1 [3:0] = Channel index 0–5 = Channel A-F Channel index for Socket

Table 77. Correctable and uncorrectable ECC error sensor event trigger offset – next steps

Event Trigger Offset		Description	Next Steps
01h	Uncorrectable ECC Error	An uncorrectable (multi-bit) ECC error has occurred. This is a fatal issue that will typically lead to an operating system crash (unless memory has been configured in a RAS mode). The system will generate a CATERR# (catastrophic error) and an MCE (Machine Check Exception Error). While the error may be due to a failing DRAM chip on the DIMM, it can also be caused by incorrect seating or improper contact between socket and DIMM, or by bent pins in the processor socket.	1. If needed, decode DIMM location from hex version of SEL. 2. Verify the DIMM is seated properly. 3. Examine gold fingers on edge of the DIMM to verify that contacts are clean. 4. Inspect the processor socket this DIMM is connected to for bent pins, and if found, replace the board. 5. Consider replacing the DIMM as a preventative measure. For multiple occurrences, replace the DIMM.
00h	Correctable ECC Error threshold reached	There have been too many (10 or more) correctable ECC errors for this particular DIMM since last boot. This event in itself does not pose any direct problems because the ECC errors are still being corrected. Depending on the RAS configuration of the memory, the IMC may take the affected DIMM offline.	Even though this event doesn't immediately lead to problems, it can indicate one of the DIMMs is slowly failing. If this error occurs more than once: 1. If needed, decode DIMM location from hex version of SEL. 2. Verify the DIMM is seated properly. 3. Examine gold fingers on edge of the DIMM to verify that contacts are clean. 4. Inspect the processor socket this DIMM is connected to for bent pins, and if found, replace the board. 5. Consider replacing the DIMM as a preventative measure. For multiple occurrences, replace the DIMM.

7.5.2 Memory Address Parity Error

Address Parity errors are errors detected in the memory addressing hardware. Because these affect the addressing of memory contents, they can potentially lead to the same sort of failures as ECC errors. They are logged as a distinct type of error because they affect memory addressing rather than memory contents, but otherwise they are treated exactly the same as Uncorrectable ECC Errors. Address Parity errors are logged to the BMC SEL, with Event Data to identify the failing address by channel and DIMM to the extent that it is possible to do so.

For different platforms, there are some differences in the event definition. For the following product families, refer to Table 78.

- Intel® Server Board based on Intel® Xeon® processor E5-1600/2600/4600 v2 product family
- Intel® Server Board based on Intel® Xeon® processor E5-2400 v2 product family
- Intel® Server Board based on Intel® Xeon® processor E5-2600 v3/v4 product family
- Intel® Server Board based on Intel® Xeon® processor E3-1200 v2/v3/v4 product family
- Intel® Server Board based on Intel® Xeon® processor E3-1200 v5/v6 product family
- Intel® Server Board based on Intel® Xeon Phi™ product family

Table 78. Address parity error sensor typical characteristics

Byte	Field	Description
8, 9	Generator ID	0033h = BIOS SMI Handler
11	Sensor Type	0ch = Memory
12	Sensor Number	13h
13	Event Direction and Event Type	[7] Event direction 0b = Assertion Event 1b = Deassertion Event [6:0] Event Type = 6Fh (Sensor Specific)
14	Event Data 1	[7:6] – 10b = OEM code in Event Data 2 [5:4] – 10b = OEM code in Event Data 3 [3:0] – Event Trigger Offset 3h = Command and Address Parity Error
15	Event Data 2	[7:5] – Reserved. Set to 0. [4] – Channel Information Validity Check: 0b = Channel Number in Event Data 3 Bits[4:3] is not valid 1b = Channel Number in Event Data 3 Bits[4:3] is valid [3] – DIMM Information Validity Check: 0b = DIMM Slot ID in Event Data 3 Bits[2:0] is not valid 1b = DIMM Slot ID in Event Data 3 Bits[2:0] is valid [2:0] – Error Type: 000b = Parity Error Type not known 001b = Data Parity Error (not used) 011b = Command and Address Parity Error All other values are reserved.
16	Event Data 3	[7:5] – Indicates the Processor Socket to which the DDR3 DIMM having the ECC error is attached: 0–3 = CPU1-4 All other values are reserved. [4:3] – Channel Number (if valid) on which the Parity Error occurred. This value will be indeterminate and should be ignored if ED2 Bit [4] is 0b. 0–3 = Channel A, B, C, D for CPU1 Channel E, F, G, H for CPU2 Channel J, K, L, M for CPU3 Channel N, P, R, T for CPU4 [2:0] – DIMM Slot ID (if valid) of the specific DIMM that was involved in the transaction that led to the parity error. This value will be indeterminate and should be ignored if ED2 Bit [3] is 0b. 0–2 = DIMM 1–3 on Channel All other values are reserved.

For the following product families, refer to Table 79.

- Intel® Server Board based on Intel® Xeon® Scalable processor family
- Intel® Server Board based on 2nd Gen Intel® Xeon® Scalable processor family
- Intel® Server Board based on Intel® Xeon® Platinum 9200 processor family

Table 79. Address parity error sensor typical characteristics for Intel® Server Boards based on Intel® Xeon® Scalable processor family, Intel® Server Board based on 2nd Gen Intel® Xeon® Scalable processor family, and Intel® Server Boards based on Intel® Xeon® Platinum 9200 processor family

Byte	Field	Description
8, 9	Generator ID	0033h = BIOS SMI Handler
11	Sensor Type	0ch = Memory
12	Sensor Number	13h
13	Event Direction and Event Type	[7] Event direction 0b = Assertion Event 1b = Deassertion Event [6:0] Event Type = 6Fh (Sensor Specific)
14	Event Data 1	[7:6] – 10b = OEM code in Event Data 2 [5:4] – 10b = OEM code in Event Data 3 [3:0] – Event Trigger Offset 3h = Command and Address Parity Error
15	Event Data 2	[7:4] – DIMM index 0-x = DIMM index per Channel [3:0] – reserved
16	Event Data 3	[7:4] – Socket index 0–3 = CPU1-4 [3:0] – Channel index 0-x = Channel index for Socket

7.5.2.1 Memory Address Parity Error Sensor – Next Steps

These are bit errors that are detected in the memory addressing hardware. An Address Parity Error implies that the memory address transmitted to the DIMM addressing circuitry has been compromised, and data read or written is compromised in turn. An Address Parity Error is logged as such in SEL but, in all other ways, is treated the same as an Uncorrectable ECC Error.

While the error may be due to a failing DRAM chip on the DIMM, it can also be caused by incorrect seating or improper contact between the socket and DIMM, or by the bent pins in the processor socket.

1. If needed, decode DIMM location from hex version of SEL.
2. Verify the DIMM is seated properly.
3. Examine gold fingers on edge of the DIMM to verify that contacts are clean.
4. Inspect the processor socket this DIMM is connected to for bent pins, and if found, replace the board.
5. Consider replacing the DIMM as a preventative measure. For multiple occurrences, replace the DIMM.

7.6 Memory Error Extension

This sensor is for capture runtime PPR failures during BIOS memory handling. This sensor generates a SEL log to determine system behavior or DIMM FRU replacement needs.

Table 80. Memory Error Extension sensor typical characteristics

Byte	Field	Description
8, 9	Generator ID	0033h = BIOS SMI Handler
11	Sensor Type	0Ch = Memory
12	Sensor Number	10h
13	Event Direction and Event Type	[7] Event direction 0b = Assertion Event 1b = Deassertion Event [6:0] Event Type = 7Fh (OEM Discrete)
14	Event Data 1	[7:6] – 10b = OEM code in Event Data 2 [5:4] – 10b = OEM code in Event Data 3 [3:0] – Event Trigger Offset 1h = Post Package Repair Runtime Request 2h = Post Package Repair Runtime Request Failure – queue limit reached
15	Event Data 2	ED2 = [7:4] = DIMM index 0–1= DIMM 1–2, DIMM index per channel [3:0] = Rank index Physical rank index per DIMM As described in Table 91
16	Event Data 3	ED3 = [7:4] = Socket index 0–3= CPU1-4 [3:0] = Channel index 0–5 = Channel A-F, Channel index for Socket As described in Table 92

7.7 ADDDC Error Sensor

ADDDC is new memory RAS feature. It supports x4 DIMM and is enabled by default when x4 DIMM plugged in. ADDDC can do bank level VLS (Virtual Lockstep), and rank VLS. ADDDC works on channel level granularity. On single rank, it has a maximum tolerance of three hard errors. There are several factors that impact VLS create. Rank number on channel, ADDDC region number, and failed error location are the three most likely factors. Skylake standard RAS SKU has one ADDDDC region per channel and can only support bank level VLS. Advance RAS SKU has two ADDDC regions per channel and can support bank, rank level VLS.

For any error introduced by ADDDC action, BIOS logs an SEL event as follows.

Table 81. ADDDC Error sensor typical characteristics

Byte	Field	Description
8, 9	Generator ID	0033h = BIOS SMI Handler
11	Sensor Type	0Ch = Memory
12	Sensor Number	20h
13	Event Direction and Event Type	[7] Event direction 0b = Assertion Event 1b = Deassertion Event [6:0] Event Type = 6Fh (Sensor-Specific)
14	Event Data 1	[7:6] – 11b = OEM code in Event Data 2 [5:4] – 11b = OEM code in Event Data 3 [3:0] – Event Trigger Offset 0h = Fully redundant 1h = Redundancy degraded
15	Event Data 2	ED2 = [7:4] = DIMM index 0–1= DIMM 1–2, DIMM index per channel [3:0] = Rank index Physical rank index per DIMM As described in Table 91
16	Event Data 3	ED3 = [7:4] = Socket index 0–3= CPU1-4 [3:0] = Channel index 0–5 = Channel A-F, Channel index for Socket As described in Table 92

8. PCI Express (PCIe*) and Legacy PCI Subsystem

The *PCI Express (PCIe*) Specification* defines standard error types under the Advanced Error Reporting (AER) capabilities. The BIOS logs AER events into the SEL.

The *Legacy PCI Specification* error types are parity error (PERR) and system error (SERR). These errors are supported and logged into the SEL.

8.1 Legacy PCI Errors

Legacy PCI errors include PERR and SERR; both are fatal errors.

Table 82. Legacy PCI error sensor typical characteristics

Byte	Field	Description
8, 9	Generator ID	0033h = BIOS SMI Handler
11	Sensor Type	13h = Critical Interrupt
12	Sensor Number	03h
13	Event Direction and Event Type	[7] Event direction 0b = Assertion Event 1b = Deassertion Event [6:0] Event Type = 6Fh (Sensor Specific)
14	Event Data 1	[7:6] – 10b = OEM code in Event Data 2 [5:4] – 10b = OEM code in Event Data 3 [3:0] – Event Trigger Offset 4h = PCI PERR 5h = PCI SERR
15	Event Data 2	PCI Bus number
16	Event Data 3	[7:3] – PCI Device number [2:0] – PCI Function number

8.1.1 Legacy PCI Error Sensor – Next Steps

1. Decode the bus, device, and function to identify the card.
2. If this is an add-in card:
   a. Verify the card is inserted properly.
   b. Install the card in another slot and check whether the error follows the card or stays with the slot.
   c. Update all firmware and drivers, including non-Intel components.
3. If this is an onboard device:
   a. Update all BIOS, firmware, and drivers.
   b. Replace the board.

8.2 PCIe* Errors

PCIe* error events are either correctable (informational event) or fatal. In both cases information is logged to help identify the source of the PCIe error and the bus, device, and function is included in the extended data fields. The PCIe devices are mapped in the operating system by bus, device, and function. Each device is uniquely identified by the bus, device, and function. PCIe device information can be found in the operating system.

8.2.1 PCIe* Fatal Errors and Fatal Error #2

When a PCIe fatal error is reported to the BIOS SMI handler, it records the error as shown in Table 83.

Table 83. PCIe* fatal error sensor typical characteristics

Byte	Field	Description
8, 9	Generator ID	0033h = BIOS SMI Handler
11	Sensor Type	13h = Critical Interrupt
12	Sensor Number	04h
13	Event Direction and Event Type	[7] Event direction 0b = Assertion Event 1b = Deassertion Event [6:0] Event Type = 70h (OEM Specific)
14	Event Data 1	[7:6] – 10b = OEM code in Event Data 2 [5:4] – 10b = OEM code in Event Data 3 [3:0] – Event Trigger 0h = Data Link Layer Protocol Error 1h = Surprise Link Down Error 2h = Completer Abort 3h = Unsupported Request 4h = Poisoned TLP 5h = Flow Control Protocol 6h = Completion Timeout 7h = Receiver Buffer Overflow 8h = ACS Violation 9h = Malformed TLP Ah = ECRC Error Bh = Received Fatal Message From Downstream Ch = Unexpected Completion Dh = Received ERR_NONFATAL Message Eh = Uncorrectable Internal Fh = MC Blocked TLP
15	Event Data 2	PCI Bus number
16	Event Data 3	[7:3] – PCI Device number [2:0] – PCI Function number

The PCIe Fatal Error #2 is a continuation of the PCIe Fatal Error.

Table 84. PCIe* Fatal Error #2 sensor typical characteristics

Byte	Field	Description
8, 9	Generator ID	0033h = BIOS SMI Handler
11	Sensor Type	13h = Critical Interrupt
12	Sensor Number	14h
13	Event Direction and Event Type	[7] Event direction 0b = Assertion Event 1b = Deassertion Event [6:0] Event Type = 76h (OEM Specific)
14	Event Data 1	[7:6] – 10b = OEM code in Event Data 2 [5:4] – 10b = OEM code in Event Data 3 [3:0] – Event Trigger Offset 0h = Atomic Egress Blocked 1h = TLP Prefix Blocked Fh = Unspecified Non-AER Fatal Error
15	Event Data 2	PCI Bus number
16	Event Data 3	[7:3] – PCI Device number [2:0] – PCI Function number

8.2.1.1 PCIe* Fatal Error and Fatal Error #2 Sensor – Next Steps

1. Decode the bus, device, and function to identify the card.
2. If this is an add-in card:
   a. Verify the card is inserted properly.
   b. Install the card in another slot and check if the error follows the card or stays with the slot.
   c. Update all firmware and drivers, including non-Intel components.
3. If this is an onboard device:
   a. Update all BIOS, firmware, and drivers.
   b. Replace the board.

8.2.2 PCIe* Correctable Errors

When a PCIe correctable error is reported to the BIOS SMI handler, it records the error as shown in Table 85.

Table 85. PCIe* correctable error sensor typical characteristics

Byte	Field	Description
8, 9	Generator ID	0033h = BIOS SMI Handler
11	Sensor Type	13h = Critical Interrupt
12	Sensor Number	05h
13	Event Direction and Event Type	[7] Event direction 0b = Assertion Event 1b = Deassertion Event [6:0] Event Type = 71h (OEM Specific)
14	Event Data 1	[7:6] – 10b = OEM code in Event Data 2 [5:4] – 10b = OEM code in Event Data 3 [3:0] – Event Trigger Offset 0h = Receiver Error 1h = Bad DLLP 2h = Bad TLP 3h = Replay Num Rollover 4h = Replay Timer timeout 5h = Advisory Non-fatal 6h = Link BW Changed 7h = Correctable Internal 8h = Header Log Overflow
15	Event Data 2	PCI Bus number
16	Event Data 3	[7:3] – PCI Device number [2:0] – PCI Function number

8.2.2.1 PCIe* Correctable Error Sensor – Next Steps

This is an informational event only. Correctable errors are acceptable and normal at a low rate of occurrence. If the error continues:

1. Decode the bus, device, and function to identify the card.
2. If this is an add-in card:
   a. Verify the card is inserted properly.
   b. Install the card in another slot and check if the error follows the card or stays with the slot.
   c. Update all firmware and drivers, including non-Intel components.
3. If this is an onboard device:
   a. Update all BIOS, firmware, and drivers.
   b. Replace the board.

9. System BIOS Events

There are a number of events that are owned by the system BIOS. These events can occur during Power On Self-Test (POST) or when coming out of a sleep state. Not all of these events signify errors. Some events are described in other chapters in this document (for example, memory events).

9.1 System Firmware Progress (Formerly POST Error)

The BIOS logs any POST errors to the SEL. The two-byte POST code gets logged in the ED2 and ED3 bytes in the SEL entry. This event is not logged every time a POST error is displayed. Even though this event indicates an error, it may not be a fatal error. If this is a serious error, there is typically also a corresponding SEL entry logged for whatever was the cause of the error; this event may contain more information about what happened than the POST error event.

Table 86. POST error sensor typical characteristics

Byte	Field	Description	
8, 9	Generator ID	0001h = BIOS POST	
11	Sensor Type	0Fh = System Firmware Progress (formerly POST Error)	
12	Sensor Number	06h	
13	Event Direction and Event Type	[7] Event direction 0b = Assertion Event 1b = Deassertion Event [6:0] Event Type = 6Fh (Sensor Specific)	
14	Event Data 1	[7:6] – 10b = OEM code in Event Data 2 [5:4] – 10b = OEM code in Event Data 3 [3:0] – Event Trigger Offset = 0h	[7:6] – 10b = OEM code in Event Data 2 [5:4] – 10b = OEM code in Event Data 3 [3:0] – Event Trigger Offset 1h = Advanced Memory Test Error 2h = Post Package Repair Finish 3h = Post Package Repair Failure
15	Event Data 2	Low Byte of POST Error Code	ED2 = [7:4] = DIMM index 0–1= DIMM 1–2, DIMM index per channel [3:0] = Rank index Physical rank index per DIMM As described in Table 91
16	Event Data 3	High Byte of POST Error Code	ED3 = [7:4] = Socket index 0–3= CPU1-4 [3:0] = Channel index 0–5 = Channel A-F, Channel index for Socket As described in Table 92

9.1.1 System Firmware Progress (Formerly POST Error) – Next Steps

See the following table for POST Error Codes.

Table 87. POST error codes for S7200AP/S7200APR, S1200SP, S2600WT/S2600WTR, S2600CW/S2600CWR, S2600KP/S2600KPR, S2600TP/S2600TPR

Error Code	Error Message	Response
0012	System RTC date/time not set	Major
0048	Password check failed	Major
0140	PCI component encountered a PERR error	Major
0141	PCI resource conflict	Major
0146	PCI out of resources error	Major
0191	Processor core/thread count mismatch detected	Fatal
0192	Processor cache size mismatch detected	Fatal
0194	Processor family mismatch detected	Fatal
0195	Processor Intel® QPI link frequencies unable to synchronize	Fatal
0196	Processor model mismatch detected	Fatal
0197	Processor frequencies unable to synchronize	Fatal
5220	BIOS Settings reset to default settings	Major
5221	Passwords cleared by jumper	Major
5224	Password clear jumper is Set	Major
8130	Processor 01 disabled	Major
8131	Processor 02 disabled	Major
8132	Processor 03 disabled	Major
8133	Processor 04 disabled	Major
8160	Processor 01 unable to apply microcode update	Major
8161	Processor 02 unable to apply microcode update	Major
8162	Processor 03 unable to apply microcode update	Major
8163	Processor 04 unable to apply microcode update	Major
8170	Processor 01 failed Self-Test (BIST)	Major
8171	Processor 02 failed Self-Test (BIST)	Major
8172	Processor 03 failed Self-Test (BIST)	Major
8173	Processor 04 failed Self-Test (BIST)	Major
8180	Processor 01 microcode update not found	Minor
8181	Processor 02 microcode update not found	Minor
8182	Processor 03 microcode update not found	Minor
8183	Processor 04 microcode update not found	Minor
8190	Watchdog timer failed on last boot	Major
8198	OS boot watchdog timer failure	Major
8300	Baseboard management controller failed self-test	Major
8305	Hot-Swap Controller failure	Major
83A0	Management Engine (ME) failed self-test	Major
83A1	Management Engine (ME) Failed to respond.	Major
84F2	Baseboard management controller failed to respond	Major
84F3	Baseboard management controller in update mode	Major
84F4	Sensor data record empty	Major
84FF	System event log full	Minor
8500	Memory component could not be configured in the selected RAS mode	Major

Error Code	Error Message	Response
8501	DIMM Population Error	Major
8520	DIMM_A1 failed test/initialization	Major
8521	DIMM_A2 failed test/initialization	Major
8522	DIMM_A3 failed test/initialization	Major
8523	DIMM_B1 failed test/initialization	Major
8524	DIMM_B2 failed test/initialization	Major
8525	DIMM_B3 failed test/initialization	Major
8526	DIMM_C1 failed test/initialization	Major
8527	DIMM_C2 failed test/initialization	Major
8528	DIMM_C3 failed test/initialization	Major
8529	DIMM_D1 failed test/initialization	Major
852A	DIMM_D2 failed test/initialization	Major
852B	DIMM_D3 failed test/initialization	Major
852C	DIMM_E1 failed test/initialization	Major
852D	DIMM_E2 failed test/initialization	Major
852E	DIMM_E3 failed test/initialization	Major
852F	DIMM_F1 failed test/initialization	Major
8530	DIMM_F2 failed test/initialization	Major
8531	DIMM_F3 failed test/initialization	Major
8532	DIMM_G1 failed test/initialization	Major
8533	DIMM_G2 failed test/initialization	Major
8534	DIMM_G3 failed test/initialization	Major
8535	DIMM_H1 failed test/initialization	Major
8536	DIMM_H2 failed test/initialization	Major
8537	DIMM_H3 failed test/initialization	Major
8538	DIMM_J1 failed test/initialization	Major
8539	DIMM_J2 failed test/initialization	Major
853A	DIMM_J3 failed test/initialization	Major
853B	DIMM_K1 failed test/initialization	Major
853C	DIMM_K2 failed test/initialization	Major
853D	DIMM_K3 failed test/initialization	Major
853E	DIMM_L1 failed test/initialization	Major
853F (Go to 85C0)	DIMM_L2 failed test/initialization	Major
8540	DIMM_A1 disabled	Major
8541	DIMM_A2 disabled	Major
8542	DIMM_A3 disabled	Major
8543	DIMM_B1 disabled	Major
8544	DIMM_B2 disabled	Major
8545	DIMM_B3 disabled	Major
8546	DIMM_C1 disabled	Major
8547	DIMM_C2 disabled	Major
8548	DIMM_C3 disabled	Major
8549	DIMM_D1 disabled	Major
854A	DIMM_D2 disabled	Major
854B	DIMM_D3 disabled	Major
854C	DIMM_E1 disabled	Major

Error Code	Error Message	Response
854D	DIMM_E2 disabled	Major
854E	DIMM_E3 disabled	Major
854F	DIMM_F1 disabled	Major
8550	DIMM_F2 disabled	Major
8551	DIMM_F3 disabled	Major
8552	DIMM_G1 disabled	Major
8553	DIMM_G2 disabled	Major
8554	DIMM_G3 disabled	Major
8555	DIMM_H1 disabled	Major
8556	DIMM_H2 disabled	Major
8557	DIMM_H3 disabled	Major
8558	DIMM_J1 disabled	Major
8559	DIMM_J2 disabled	Major
855A	DIMM_J3 disabled	Major
855B	DIMM_K1 disabled	Major
855C	DIMM_K2 disabled	Major
855D	DIMM_K3 disabled	Major
855E	DIMM_L1 disabled	Major
855F (Go to 85D0)	DIMM_L2 disabled	Major
8560	DIMM_A1 encountered a Serial Presence Detection (SPD) failure	Major
8561	DIMM_A2 encountered a Serial Presence Detection (SPD) failure	Major
8562	DIMM_A3 encountered a Serial Presence Detection (SPD) failure	Major
8563	DIMM_B1 encountered a Serial Presence Detection (SPD) failure	Major
8564	DIMM_B2 encountered a Serial Presence Detection (SPD) failure	Major
8565	DIMM_B3 encountered a Serial Presence Detection (SPD) failure	Major
8566	DIMM_C1 encountered a Serial Presence Detection (SPD) failure	Major
8567	DIMM_C2 encountered a Serial Presence Detection (SPD) failure	Major
8568	DIMM_C3 encountered a Serial Presence Detection (SPD) failure	Major
8569	DIMM_D1 encountered a Serial Presence Detection (SPD) failure	Major
856A	DIMM_D2 encountered a Serial Presence Detection (SPD) failure	Major
856B	DIMM_D3 encountered a Serial Presence Detection (SPD) failure	Major
856C	DIMM_E1 encountered a Serial Presence Detection (SPD) failure	Major
856D	DIMM_E2 encountered a Serial Presence Detection (SPD) failure	Major
856E	DIMM_E3 encountered a Serial Presence Detection (SPD) failure	Major
856F	DIMM_F1 encountered a Serial Presence Detection (SPD) failure	Major
8570	DIMM_F2 encountered a Serial Presence Detection (SPD) failure	Major
8571	DIMM_F3 encountered a Serial Presence Detection (SPD) failure	Major
8572	DIMM_G1 encountered a Serial Presence Detection (SPD) failure	Major
8573	DIMM_G2 encountered a Serial Presence Detection (SPD) failure	Major
8574	DIMM_G3 encountered a Serial Presence Detection (SPD) failure	Major
8575	DIMM_H1 encountered a Serial Presence Detection (SPD) failure	Major
8576	DIMM_H2 encountered a Serial Presence Detection (SPD) failure	Major
8577	DIMM_H3 encountered a Serial Presence Detection (SPD) failure	Major
8578	DIMM_J1 encountered a Serial Presence Detection (SPD) failure	Major
8579	DIMM_J2 encountered a Serial Presence Detection (SPD) failure	Major
857A	DIMM_J3 encountered a Serial Presence Detection (SPD) failure	Major

Error Code	Error Message	Response
857B	DIMM_K1 encountered a Serial Presence Detection (SPD) failure	Major
857C	DIMM_K2 encountered a Serial Presence Detection (SPD) failure	Major
857D	DIMM_K3 encountered a Serial Presence Detection (SPD) failure	Major
857E	DIMM_L1 encountered a Serial Presence Detection (SPD) failure	Major
857F (Go to 85E0)	DIMM_L2 encountered a Serial Presence Detection (SPD) failure	Major
85C0	DIMM_L3 failed test/initialization	Major
85C1	DIMM_M1 failed test/initialization	Major
85C2	DIMM_M2 failed test/initialization	Major
85C3	DIMM_M3 failed test/initialization	Major
85C4	DIMM_N1 failed test/initialization	Major
85C5	DIMM_N2 failed test/initialization	Major
85C6	DIMM_N3 failed test/initialization	Major
85C7	DIMM_P1 failed test/initialization	Major
85C8	DIMM_P2 failed test/initialization	Major
85C9	DIMM_P3 failed test/initialization	Major
85CA	DIMM_R1 failed test/initialization	Major
85CB	DIMM_R2 failed test/initialization	Major
85CC	DIMM_R3 failed test/initialization	Major
85CD	DIMM_T1 failed test/initialization	Major
85CE	DIMM_T2 failed test/initialization	Major
85CF	DIMM_T3 failed test/initialization	Major
85D0	DIMM_L3 disabled	Major
85D1	DIMM_M1 disabled	Major
85D2	DIMM_M2 disabled	Major
85D3	DIMM_M3 disabled	Major
85D4	DIMM_N1 disabled	Major
85D5	DIMM_N2 disabled	Major
85D6	DIMM_N3 disabled	Major
85D7	DIMM_P1 disabled	Major
85D8	DIMM_P2 disabled	Major
85D9	DIMM_P3 disabled	Major
85DA	DIMM_R1 disabled	Major
85DB	DIMM_R2 disabled	Major
85DC	DIMM_R3 disabled	Major
85DD	DIMM_T1 disabled	Major
85DE	DIMM_T2 disabled	Major
85DF	DIMM_T3 disabled	Major
85E0	DIMM_L3 encountered a Serial Presence Detection (SPD) failure	Major
85E1	DIMM_M1 encountered a Serial Presence Detection (SPD) failure	Major
85E2	DIMM_M2 encountered a Serial Presence Detection (SPD) failure	Major
85E3	DIMM_M3 encountered a Serial Presence Detection (SPD) failure	Major
85E4	DIMM_N1 encountered a Serial Presence Detection (SPD) failure	Major
85E5	DIMM_N2 encountered a Serial Presence Detection (SPD) failure	Major
85E6	DIMM_N3 encountered a Serial Presence Detection (SPD) failure	Major
85E7	DIMM_P1 encountered a Serial Presence Detection (SPD) failure	Major
85E8	DIMM_P2 encountered a Serial Presence Detection (SPD) failure	Major

Error Code	Error Message	Response
85E9	DIMM_P3 encountered a Serial Presence Detection (SPD) failure	Major
85EA	DIMM_R1 encountered a Serial Presence Detection (SPD) failure	Major
85EB	DIMM_R2 encountered a Serial Presence Detection (SPD) failure	Major
85EC	DIMM_R3 encountered a Serial Presence Detection (SPD) failure	Major
85ED	DIMM_T1 encountered a Serial Presence Detection (SPD) failure	Major
85EE	DIMM_T2 encountered a Serial Presence Detection (SPD) failure	Major
85EF	DIMM_T3 encountered a Serial Presence Detection (SPD) failure	Major
8604	POST Reclaim of non-critical NVRAM variables	Minor
8605	BIOS Settings are corrupted	Major
8606	NVRAM variable space was corrupted and has been reinitialized	Major
92A3	Serial port component was not detected	Major
92A9	Serial port component encountered a resource conflict error	Major
A000	TPM device not detected.	Minor
A001	TPM device missing or not responding.	Minor
A002	TPM device failure.	Minor
A003	TPM device failed self-test.	Minor
A100	BIOS ACM Error	Major
A421	PCI component encountered a SERR error	Fatal
A5A0	PCI Express component encountered a PERR error	Minor
A5A1	PCI Express component encountered an SERR error	Fatal
A6A0	DXE Boot Services driver: Not enough memory available to shadow a Legacy Option ROM.	Minor

Table 88. POST error codes for S2600BP/S2600BPR, S2600WF/S2600WFR, S2600ST/S2600STR/S9200WK

Error Code	Error Message	Response
0012	System RTC date/time not set	Major
0048	Password check failed	Major
0140	PCI component encountered a PERR error	Major
0141	PCI resource conflict	Major
0146	PCI out of resources error	Major
0191	Processor core/thread count mismatch detected	Fatal
0192	Processor cache size mismatch detected	Fatal
0194	Processor family mismatch detected	Fatal
0195	Processor Intel(R) UPI link frequencies unable to synchronize	Fatal
0196	Processor model mismatch detected	Fatal
0197	Processor frequencies unable to synchronize	Fatal
5220	BIOS Settings reset to default settings	Major
5221	Passwords cleared by jumper	Major
5224	Password clear jumper is Set	Major
8130	Processor 01 disabled	Major
8131	Processor 02 disabled	Major
8160	Processor 01 unable to apply microcode update	Major
8161	Processor 02 unable to apply microcode update	Major
8170	Processor 01 failed Self-Test (BIST)	Major
8171	Processor 02 failed Self-Test (BIST)	Major
8180	Processor 01 microcode update not found	Minor
8181	Processor 02 microcode update not found	Minor
8190	Watchdog timer failed on last boot.	Major
8198	OS boot watchdog timer failure.	Major
8300	Baseboard Management Controller failed self-test.	Major
8305	Hot Swap Controller failure	Major
83A0	Management Engine (ME) failed self-test.	Major
83A1	Management Engine (ME) Failed to respond.	Major
84F2	Baseboard management controller failed to respond	Major
84F3	Baseboard Management Controller in Update Mode.	Major
84F4	Baseboard Management Controller Sensor Data Record empty.	Major
84FF	System Event Log full	Minor
85FC	Memory component could not be configured in the selected RAS mode	Major
8501	Memory Population Error	Major
8520	Memory failed test/initialization CPU1_DIMM_A1	Major
8521	Memory failed test/initialization CPU1_DIMM_A2	Major
8522	Memory failed test/initialization CPU1_DIMM_A3	Major
8523	Memory failed test/initialization CPU1_DIMM_B1	Major
8524	Memory failed test/initialization CPU1_DIMM_B2	Major
8525	Memory failed test/initialization CPU1_DIMM_B3	Major
8526	Memory failed test/initialization CPU1_DIMM_C1	Major
8527	Memory failed test/initialization CPU1_DIMM_C2	Major
8528	Memory failed test/initialization CPU1_DIMM_C3	Major

Error Code	Error Message	Response
8529	Memory failed test/initialization CPU1_DIMM_D1	Major
852A	Memory failed test/initialization CPU1_DIMM_D2	Major
852B	Memory failed test/initialization CPU1_DIMM_D3	Major
852C	Memory failed test/initialization CPU1_DIMM_E1	Major
852D	Memory failed test/initialization CPU1_DIMM_E2	Major
852E	Memory failed test/initialization CPU1_DIMM_E3	Major
852F	Memory failed test/initialization CPU1_DIMM_F1	Major
8530	Memory failed test/initialization CPU1_DIMM_F2	Major
8531	Memory failed test/initialization CPU1_DIMM_F3	Major
8532	Memory failed test/initialization CPU1_DIMM_G1	Major
8533	Memory failed test/initialization CPU1_DIMM_G2	Major
8534	Memory failed test/initialization CPU1_DIMM_G3	Major
8535	Memory failed test/initialization CPU1_DIMM_H1	Major
8536	Memory failed test/initialization CPU1_DIMM_H2	Major
8537	Memory failed test/initialization CPU1_DIMM_H3	Major
8538	Memory failed test/initialization CPU2_DIMM_A1	Major
8539	Memory failed test/initialization CPU2_DIMM_A2	Major
853A	Memory failed test/initialization CPU2_DIMM_A3	Major
853B	Memory failed test/initialization CPU2_DIMM_B1	Major
853C	Memory failed test/initialization CPU2_DIMM_B2	Major
853D	Memory failed test/initialization CPU2_DIMM_B3	Major
853E	Memory failed test/initialization CPU2_DIMM_C1	Major
853F (Go to 85C0)	Memory failed test/initialization CPU2_DIMM_C2	Major
8540	Memory disabled.CPU1_DIMM_A1	Major
8541	Memory disabled.CPU1_DIMM_A2	Major
8542	Memory disabled.CPU1_DIMM_A3	Major
8543	Memory disabled.CPU1_DIMM_B1	Major
8544	Memory disabled.CPU1_DIMM_B2	Major
8545	Memory disabled.CPU1_DIMM_B3	Major
8546	Memory disabled.CPU1_DIMM_C1	Major
8547	Memory disabled.CPU1_DIMM_C2	Major
8548	Memory disabled.CPU1_DIMM_C3	Major
8549	Memory disabled.CPU1_DIMM_D1	Major
854A	Memory disabled.CPU1_DIMM_D2	Major
854B	Memory disabled.CPU1_DIMM_D3	Major
854C	Memory disabled.CPU1_DIMM_E1	Major
854D	Memory disabled.CPU1_DIMM_E2	Major
854E	Memory disabled.CPU1_DIMM_E3	Major
854F	Memory disabled.CPU1_DIMM_F1	Major
8550	Memory disabled.CPU1_DIMM_F2	Major
8551	Memory disabled.CPU1_DIMM_F3	Major
8552	Memory disabled.CPU1_DIMM_G1	Major
8553	Memory disabled.CPU1_DIMM_G2	Major
8554	Memory disabled.CPU1_DIMM_G3	Major
8555	Memory disabled.CPU1_DIMM_H1	Major

Error Code	Error Message	Response
8556	Memory disabled.CPU1_DIMM_H2	Major
8557	Memory disabled.CPU1_DIMM_H3	Major
8558	Memory disabled.CPU2_DIMM_A1	Major
8559	Memory disabled.CPU2_DIMM_A2	Major
855A	Memory disabled.CPU2_DIMM_A3	Major
855B	Memory disabled.CPU2_DIMM_B1	Major
855C	Memory disabled.CPU2_DIMM_B2	Major
855D	Memory disabled.CPU2_DIMM_B3	Major
855E	Memory disabled.CPU2_DIMM_C1	Major
855F (Go to 85D0)	Memory disabled.CPU2_DIMM_C2	Major
8560	Memory encountered a Serial Presence Detection(SPD) failure.CPU1_DIMM_A1	Major
8561	Memory encountered a Serial Presence Detection(SPD) failure.CPU1_DIMM_A2	Major
8562	Memory encountered a Serial Presence Detection(SPD) failure.CPU1_DIMM_A3	Major
8563	Memory encountered a Serial Presence Detection(SPD) failure.CPU1_DIMM_B1	Major
8564	Memory encountered a Serial Presence Detection(SPD) failure.CPU1_DIMM_B2	Major
8565	Memory encountered a Serial Presence Detection(SPD) failure.CPU1_DIMM_B3	Major
8566	Memory encountered a Serial Presence Detection(SPD) failure.CPU1_DIMM_C1	Major
8567	Memory encountered a Serial Presence Detection (SPD) failure.CPU1_DIMM_C2	Major
8568	Memory encountered a Serial Presence Detection (SPD) failure.CPU1_DIMM_C3	Major
8569	Memory encountered a Serial Presence Detection(SPD) failure.CPU1_DIMM_D1	Major
856A	Memory encountered a Serial Presence Detection(SPD) failure.CPU1_DIMM_D2	Major
856B	Memory encountered a Serial Presence Detection(SPD) failure.CPU1_DIMM_D3	Major
856C	Memory encountered a Serial Presence Detection(SPD) failure.CPU1_DIMM_E1	Major
856D	Memory encountered a Serial Presence Detection(SPD) failure.CPU1_DIMM_E2	Major
856E	Memory encountered a Serial Presence Detection(SPD) failure.CPU1_DIMM_E3	Major
856F	Memory encountered a Serial Presence Detection(SPD) failure.CPU1_DIMM_F1	Major
8570	Memory encountered a Serial Presence Detection(SPD) failure.CPU1_DIMM_F2	Major
8571	Memory encountered a Serial Presence Detection(SPD) failure.CPU1_DIMM_F3	Major
8572	Memory encountered a Serial Presence Detection(SPD) failure.CPU1_DIMM_G1	Major
8573	Memory encountered a Serial Presence Detection(SPD) failure.CPU1_DIMM_G2	Major
8574	Memory encountered a Serial Presence Detection(SPD) failure.CPU1_DIMM_G3	Major
8575	Memory encountered a Serial Presence Detection(SPD) failure.CPU1_DIMM_H1	Major
8576	Memory encountered a Serial Presence Detection(SPD) failure.CPU1_DIMM_H2	Major
8577	Memory encountered a Serial Presence Detection(SPD) failure.CPU1_DIMM_H3	Major
8578	Memory encountered a Serial Presence Detection(SPD) failure.CPU2_DIMM_A1	Major
8579	Memory encountered a Serial Presence Detection(SPD) failure.CPU2_DIMM_A2	Major
857A	Memory encountered a Serial Presence Detection(SPD) failure.CPU2_DIMM_A3	Major
857B	Memory encountered a Serial Presence Detection(SPD) failure.CPU2_DIMM_B1	Major
857C	Memory encountered a Serial Presence Detection(SPD) failure.CPU2_DIMM_B2	Major
857D	Memory encountered a Serial Presence Detection(SPD) failure.CPU2_DIMM_B3	Major
857E	Memory encountered a Serial Presence Detection(SPD) failure.CPU2_DIMM_C1	Major
857F (Go to 85E0)	Memory encountered a Serial Presence Detection(SPD) failure.CPU2_DIMM_C2	Major
85C0	Memory failed test/initialization CPU2_DIMM_C3	Major
85C1	Memory failed test/initialization CPU2_DIMM_D1	Major

Error Code	Error Message	Response
85C2	Memory failed test/initialization CPU2_DIMM_D2	Major
85C3	Memory failed test/initialization CPU2_DIMM_D3	Major
85C4	Memory failed test/initialization CPU2_DIMM_E1	Major
85C5	Memory failed test/initialization CPU2_DIMM_E2	Major
85C6	Memory failed test/initialization CPU2_DIMM_E3	Major
85C7	Memory failed test/initialization CPU2_DIMM_F1	Major
85C8	Memory failed test/initialization CPU2_DIMM_F2	Major
85C9	Memory failed test/initialization CPU2_DIMM_F3	Major
85CA	Memory failed test/initialization CPU2_DIMM_G1	Major
85CB	Memory failed test/initialization CPU2_DIMM_G2	Major
85CC	Memory failed test/initialization CPU2_DIMM_G3	Major
85CD	Memory failed test/initialization CPU2_DIMM_H1	Major
85CE	Memory failed test/initialization CPU2_DIMM_H2	Major
85CF	Memory failed test/initialization CPU2_DIMM_H3	Major
85D0	Memory disabled.CPU2_DIMM_C3	Major
85D1	Memory disabled.CPU2_DIMM_D1	Major
85D2	Memory disabled.CPU2_DIMM_D2	Major
85D3	Memory disabled.CPU2_DIMM_D3	Major
85D4	Memory disabled.CPU2_DIMM_E1	Major
85D5	Memory disabled.CPU2_DIMM_E2	Major
85D6	Memory disabled.CPU2_DIMM_E3	Major
85D7	Memory disabled.CPU2_DIMM_F1	Major
85D8	Memory disabled.CPU2_DIMM_F2	Major
85D9	Memory disabled.CPU2_DIMM_F3	Major
85DA	Memory disabled.CPU2_DIMM_G1	Major
85DB	Memory disabled.CPU2_DIMM_G2	Major
85DC	Memory disabled.CPU2_DIMM_G3	Major
85DD	Memory disabled.CPU2_DIMM_H1	Major
85DE	Memory disabled.CPU2_DIMM_H2	Major
85DF	Memory disabled.CPU2_DIMM_H3	Major
85E0	Memory encountered a Serial Presence Detection(SPD) failure.CPU2_DIMM_C3	Major
85E1	Memory encountered a Serial Presence Detection (SPD) failure. CPU2_DIMM_D1	Major
85E2	Memory encountered a Serial Presence Detection (SPD) failure.CPU2_DIMM_D2	Major
85E3	Memory encountered a Serial Presence Detection(SPD) failure.CPU2_DIMM_D3	Major
85E4	Memory encountered a Serial Presence Detection(SPD) failure.CPU2_DIMM_E1	Major
85E5	Memory encountered a Serial Presence Detection(SPD) failure.CPU2_DIMM_E2	Major
85E6	Memory encountered a Serial Presence Detection(SPD) failure.CPU2_DIMM_E3	Major
85E7	Memory encountered a Serial Presence Detection (SPD) failure.CPU2_DIMM_F1	Major
85E8	Memory encountered a Serial Presence Detection(SPD) failure.CPU2_DIMM_F2	Major
85E9	Memory encountered a Serial Presence Detection(SPD) failure.CPU2_DIMM_F3	Major
85EA	Memory encountered a Serial Presence Detection(SPD) failure.CPU2_DIMM_G1	Major
85EB	Memory encountered a Serial Presence Detection(SPD) failure. CPU2_DIMM_G2	Major
85EC	Memory encountered a Serial Presence Detection(SPD) failure.CPU2_DIMM_G3	Major
85ED	Memory encountered a Serial Presence Detection(SPD) failure.CPU2_DIMM_H1	Major
85EE	Memory encountered a Serial Presence Detection(SPD) failure.CPU2_DIMM_H2	Major
85EF	Memory encountered a Serial Presence Detection(SPD) failure.CPU2_DIMM_H3	Major

Error Code	Error Message	Response
8604	POST Reclaim of non-critical NVRAM variables	Minor
8605	BIOS Settings are corrupted	Major
8606	NVRAM variable space was corrupted and has been reinitialized	Major
8607	Recovery boot has been initiated. **Note**: The Primary BIOS image may be corrupted or the system may hang during POST. A BIOS update is required.	Fatal
A100	BIOS ACM Error	Major
A421	PCI component encountered a SERR error	Fatal
A5A0	PCI Express component encountered a PERR error	Minor
A5A1	PCI Express component encountered an SERR error	Fatal
A6A0	DXE Boot Services driver: Not enough memory available to shadow a Legacy Option ROM.	Minor

9.2 BIOS Recovery

These events are related to the BIOS Recovery feature and information only. *BIOS Release Notes* records the detailed recovery procedures.

When BIOS Recovery Boot Jumper is set, the BIOS begins with a 'Recovery Start' event logged to the SEL, loads and boots with the Backup BIOS image inside the BIOS flash itself. This process takes place before any video or console is available. The system boots into the shell directly while a 'Recovery Complete' SEL logged. Follow BIOS update under recovery mode manually.

Table 89. BIOS recovery sensor typical characteristics

Byte	Field	Description
8, 9	Generator ID	0033h = BIOS SMI Handler
11	Sensor Type	0Fh = System Firmware Progress (formerly POST Error)
12	Sensor Number	15h
13	Event Direction and Event Type	[7] Event direction 0b = Assertion Event 1b = Deassertion Event [6:0] Event Type 70h (OEM Discrete) for BIOS Recovery Start F0h (OEM Discrete) for BIOS Recovery Complete
14	Event Data 1	[7:6] – 00b = OEM code in Event Data 2 [5:4] – 00b = OEM code in Event Data 3 [3:0] – Event Trigger Offset 1h = BIOS Recovery Start (Event Type = 0x70) 1h = BIOS Recovery Complete (Event Type = 0xF0)
15	Event Data 2	Not used
16	Event Data 3	Not used

9.3 OEM BIOS POST Event

This sensor adds one additional type and log Advanced Memory Test results in SEL.

Table 90. OEM BIOS POST Event typical characteristics

Byte	Field	Description
8, 9	Generator ID	0001h = BIOS POST
11	Sensor Type	12h (System Event)
12	Sensor Number	10h
13	Event Direction and Event Type	[7] Event direction 0b = Assertion Event 1b = Deassertion Event [6:0] Event Type = 7Fh (OEM Discrete)
14	Event Data 1	[7:6] – 10b = OEM code in Event Data 2 [5:4] – 10b = OEM code in Event Data 3 [3:0] – Event Trigger Offset 4h = Advanced Memory Test Completion without Error 5h = Advanced Memory Test Completion with Error
15	Event Data 2	ED2 = [7:4] = DIMM index 0–1= DIMM 1–2, DIMM index per channel [3:0] = Rank index Physical rank index per DIMM As described in Table 91
16	Event Data 3	ED3 = [7:4] = Socket index 0–3= CPU1-4 [3:0] = Channel index 0–5 = Channel A-F, Channel index for Socket As described in Table 92 and Table 30.

Table 91. ED2 detail for DIMM and RANK

ED2	DIMM	RANK
0x00	DIMM 1	RANK 0
0x01	DIMM 1	RANK 1
0x02	DIMM 1	RANK 2
0x03	DIMM 1	RANK 3
0x10	DIMM 2	RANK 0
0x11	DIMM 2	RANK 1
0x12	DIMM 2	RANK 2
0x13	DIMM 2	RANK 3

Table 92. ED3 detail for CPU and Memory Channel

ED3	DIMM	RANK
0x00	CPU 1	Channel A
0x01	CPU 1	Channel B
0x02	CPU 1	Channel C
0x03	CPU 1	Channel D
0x04	CPU 1	Channel E
0x05	CPU 1	Channel F
0x10	CPU 2	Channel A
0x11	CPU 2	Channel B
0x12	CPU 2	Channel C
0x13	CPU 2	Channel D
0x14	CPU 2	Channel E
0x15	CPU 2	Channel F
0x20	CPU 3	Channel A
0x21	CPU 3	Channel B
0x22	CPU 3	Channel C
0x23	CPU 3	Channel D
0x24	CPU 3	Channel E
0x25	CPU 3	Channel F
0x30	CPU 4	Channel A
0x31	CPU 4	Channel B
0x32	CPU 4	Channel C
0x33	CPU 4	Channel D
0x34	CPU 4	Channel E
0x35	CPU 4	Channel F

10. Chassis Subsystem

The BMC monitors several aspects of the chassis. Next to logging when the power and reset buttons get pressed, the BMC also monitors chassis intrusion if a chassis intrusion switch is included in the chassis, as well as looking at the network connections, and logging an event whenever the physical network link is lost.

10.1 Physical Security

Two sensors are included in the physical security subsystem: chassis intrusion and LAN leash lost.

10.1.1 Chassis Intrusion

Chassis Intrusion is monitored on supported chassis, and the BMC logs corresponding events when the chassis lid is opened and closed.

10.1.2 LAN Leash Lost

The LAN Leash lost sensor monitors the physical connection on the onboard network ports. If a LAN Leash lost event is logged, this means the network port lost its physical connection.

Table 93. Physical security sensor typical characteristics

Byte	Field	Description
11	Sensor Type	05h = Physical Security
12	Sensor Number	04h
13	Event Direction and Event Type	[7] Event direction 0b = Assertion Event 1b = Deassertion Event [6:0] Event Type = 6Fh (Sensor Specific)
14	Event Data 1	[7:6] – 00b = Unspecified Event Data 2 [5:4] – 00b = Unspecified Event Data 3 [3:0] – Event Trigger Offset as described in Table 94
15	Event Data 2	Not used
16	Event Data 3	Not used

Table 94. Physical security sensor event trigger offset – next steps

Event Trigger Offset		Description	Next Steps
00h	Chassis intrusion	The chassis has been opened (or the chassis intrusion sensor is not connected).	1. Use the Quick Start Guide and the Service Guide to determine whether the chassis intrusion switch is connected properly. 2. If this is the case, make sure it makes proper contact when the chassis is closed. 3. If this is also the case, someone has opened the chassis. Ensure nobody has access to the system that should not.
04h	LAN leash lost	A LAN cable that was present when the BMC initialized has been unplugged. This event gets logged when the electrical connection on the NIC connector is lost.	This is most likely due to unplugging the cable but can also happen if there is an issue with the cable or switch. 1. Check the LAN cable and connector for issues. 2. Investigate switch logs where possible. 3. Ensure nobody has access to the server that should not.

10.2 Front Panel (NMI) Interrupt

The BMC supports a non-maskable interrupt (NMI) sensor for logging an event when a diagnostic interrupt is generated for the following cases:

- The front panel diagnostic interrupt button is pressed.
- The BMC receives an IPMI Chassis Control command that requests this action.

The front panel interrupt button (also referred to as NMI button) is a recessed button on the front panel that allows the user to force a critical interrupt that causes a crash error or kernel panic.

Table 95. Front panel (NMI) interrupt sensor typical characteristics

Byte	Field	Description
11	Sensor Type	13h = Critical Interrupt
12	Sensor Number	05h
13	Event Direction and Event Type	[7] Event direction 0b = Assertion Event 1b = Deassertion Event [6:0] Event Type = 6Fh (Sensor Specific)
14	Event Data 1	[7:6] – 00b = Unspecified Event Data 2 [5:4] – 00b = Unspecified Event Data 3 [3:0] – Event Trigger Offset = 0h
15	Event Data 2	Not used
16	Event Data 3	Not used

10.2.1 Front Panel (NMI) Interrupt – Next Steps

The purpose of this button is for diagnosing software issues. When a critical interrupt is generated, the operating system typically saves a memory dump. This allows for exact analysis of what is going on in system memory, which can be useful for software developers, or for troubleshooting the operating system, software, and driver issues.

If this button was not actually pressed, ensure there is no physical fault with the front panel.

This event only gets logged if a user pressed the NMI button or sent an IPMI Chassis Control command requesting this action and, although it causes the operating system to crash, is not an error.

10.3 Button Sensor

The BMC logs when the front panel power and reset buttons get pressed. This is purely for informational purposes and these events do not indicate errors.

Table 96. Button sensor typical characteristics

Byte	Field	Description
11	Sensor Type	14h = Button/Switch
12	Sensor Number	09h
13	Event Direction and Event Type	[7] Event direction 0b = Assertion Event 1b = Deassertion Event [6:0] Event Type = 6Fh (Sensor Specific)
14	Event Data 1	[7:6] – 00b = Unspecified Event Data 2 [5:4] – 00b = Unspecified Event Data 3 [3:0] – Event Trigger Offset 0h = Power Button 2h = Reset Button
15	Event Data 2	Not used
16	Event Data 3	Not used

11. Miscellaneous Events

The miscellaneous events section addresses sensors not easily grouped with other sensor types.

11.1 IPMI Watchdog

Intel® Server Systems support an IPMI watchdog timer that can check to see whether the operating system is still responsive. The timer is disabled by default, and has to be enabled manually. It then requires an IPMI-aware utility in the operating system that resets the timer before it expires. If the timer does expire, the BMC can act if it is configured to do so (reset, power down, power cycle, or generate a critical interrupt).

Table 97. IPMI watchdog sensor typical characteristics

Byte	Field	Description
11	Sensor Type	23h = Watchdog 2
12	Sensor Number	03h
13	Event Direction and Event Type	[7] Event direction 0b = Assertion Event 1b = Deassertion Event [6:0] Event Type = 6Fh (Sensor Specific)
14	Event Data 1	[7:6] – 11B = Sensor-specific event extension code in Event Data 2 [5:4] – 00b = Unspecified Event Data 3 [3:0] – Event Trigger Offset as described in Table 98
15	Event Data 2	[7:4] – Interrupt type 0h = None 1h = SMI 2h = NMI 3h = Messaging Interrupt Fh = Unspecified All other = Reserved [3:0] – Timer use at expiration 0h = Reserved 1h = BIOS FRB2 2h = BIOS/POST 3h = Operating system Load 4h = SMS/OS 5h = OEM Fh = Unspecified All other = Reserved
16	Event Data 3	Not used

Table 98. IPMI watchdog sensor event trigger offset – next steps

Event Trigger Offset		Description	Next Steps
00h	Timer expired, status only	Intel® Server Systems support a BMC watchdog timer, which can check to see whether the operating system is still responsive. The timer is disabled by default, and has to be enabled manually. It then requires an IPMI-aware utility in the operating system that resets the timer before it expires. If the timer does expire, the BMC can act if it is configured to do so (reset, power down, power cycle, or generate a critical interrupt).	If this event is being logged, it is because the BMC has been configured to check the watchdog timer. 1. Make sure to have support for this in the operating system (typically using a third-party IPMI-aware utility such as ipmitool or ipmiutil along with the OpenIPMI driver). 2. If this is the case, it is likely the operating system has hung, and investigate operating system event logs need to be investigated to determine what may have caused this.
01h	Hard reset		
02h	Power down		
03h	Power cycle		
08h	Timer interrupt		

11.2 System Management Interrupt (SMI) Timeout

System management interrupt (SMI) is an interrupt that gets generated so the processor can service server management events (typically memory or PCI errors, or other forms of critical interrupts), in order to log them to the SEL. If this interrupt times out, the system is frozen. The BMC resets the system after logging the event.

Table 99. SMI timeout sensor typical characteristics

Byte	Field	Description
11	Sensor Type	F3h = SMI Timeout
12	Sensor Number	06h
13	Event Direction and Event Type	[7] Event direction 0b = Assertion Event 1b = Deassertion Event [6:0] Event Type = 03h (“digital” Discrete)
14	Event Data 1	[7:6] – 00b = Unspecified Event Data 2 [5:4] – 00b = Unspecified Event Data 3 [3:0] – Event Trigger Offset = 1h = State Asserted
15	Event Data 2	Not used
16	Event Data 3	Not used

11.2.1 SMI Timeout – Next Steps

This event normally only occurs after another more critical event.

1. Check the SEL for any critical interrupts, memory errors, bus errors, PCI errors, or any other serious errors.
2. If these are not present, the system locked up before it was able to log the original issue. In this case, low level debug is normally required.

11.3 System Event Log Cleared

The BMC logs an SEL clear event. This is only ever the first event in the SEL. The cause of this event is either a manual SEL clear using `selview` or some other IPMI-aware utility, or is done in the factory as one of the last steps in the manufacturing process.

This is an informational event only.

Table 100. System event log cleared sensor typical characteristics

Byte	Field	Description
11	Sensor Type	10h = Event Logging Disabled
12	Sensor Number	07h
13	Event Direction and Event Type	[7] Event direction 0b = Assertion Event 1b = Deassertion Event [6:0] Event Type = 6Fh (Sensor Specific)
14	Event Data 1	[7:6] – 00b = Unspecified Event Data 2 [5:4] – 00b = Unspecified Event Data 3 [3:0] – Event Trigger Offset = 2h = Log area reset/cleared
15	Event Data 2	Not used
16	Event Data 3	Not used

11.4 System Event Sensor

The BMC supports a System Event sensor and logs an SEL event for a Platform Event Filter (PEF) action, BIOS/Intel® ME out-of-band (OOB) update, and BIOS configuration change from the BMC embedded web server (EWS).

11.4.1 System Event – PEF Action

The BMC is configurable to send alerts for events logged into the SEL. These alerts are called Platform Event Filters (PEFs) and are disabled by default. The user must configure and enable this feature. PEF events are logged if the BMC acts due to a PEF configuration. The BMC event triggering the PEF action is also in the SEL.

This is functionality built into the BMC to allow it to send alerts (SNMP or other) for any event that gets logged to the SEL. PEF filters are turned off by default and have to be enabled manually using a deployment assistant, the Intel Server Configuration Utility, or an IPMI-aware utility.

Table 101. System event – PEF action sensor typical characteristics

Byte	Field	Description
11	Sensor Type	12h = System Event
12	Sensor Number	08h
13	Event Direction and Event Type	[7] Event direction 0b = Assertion Event 1b = Deassertion Event [6:0] Event Type = 6Fh (Sensor Specific)
14	Event Data 1	[7:6] – 11B = Sensor-specific event extension code in Event Data 2 [5:4] – 00b = Unspecified Event Data 3 [3:0] – Event Trigger Offset = 4h = PEF Action
15	Event Data 2	[7:6] – Reserved [5] – 1b = Diagnostic Interrupt (NMI) [4] – 1b = OEM action [3] – 1b = Power cycle [2] – 1b = Reset [1] – 1b = Power off [0] – 1b = Alert
16	Event Data 3	Not used

This event gets logged if the BMC takes an action due to PEF configuration. Actions can be sending an alert, along with possibly resetting, power cycling, or powering down the system. There is another event that has led to the action; investigate the SEL and PEF settings to identify this event, and troubleshoot accordingly.

11.4.2 System Event – OOB Update and BIOS Configuration Change

This event gets logged if the OOB BIOS/Intel ME update or BIOS configuration change is triggered from the BMC EWS.

Table 102. System event – BIOS/Intel® ME OOB update and BIOS Configuration change

Byte	Field	Description
11	Sensor Type	12h = System Event
12	Sensor Number	08h
13	Event Direction and Event Type	[7] Event direction 0b = Assertion Event 1b = Deassertion Event [6:0] Event Type = 6Fh (Sensor Specific)
14	Event Data 1	[7:6] - 11b = OEM code in Byte2 [5:4] - 00b = unspecified byte 3 [3:0] – 07h = image is uploaded [3:0] – 08h = image is lost
15	Event Data 2	[7:0] 00h = BIOS Configuration Table 01h = BIOS Configuration change 02h = BIOS Image 03h = ME Image 04h = FD Image
16	Event Data 3	[7:0] 00h = Firmware Update 01h = BIOS Configuration

11.5 BMC Watchdog Sensor

The BMC supports an IPMI sensor to report that a BMC reset has occurred due to an action taken by the BMC Watchdog feature. A SEL event is logged when either the BMC FW stack is reset or the BMC CPU itself is reset.

Table 103. BMC watchdog sensor typical characteristics

Byte	Field	Description
11	Sensor Type	28h = Management Subsystem Health
12	Sensor Number	0Ah
13	Event Direction and Event Type	[7] Event direction 0b = Assertion Event 1b = Deassertion Event [6:0] Event Type = 03h (“digital” Discrete)
14	Event Data 1	[7:6] – 00b = Unspecified Event Data 2 [5:4] – 00b = Unspecified Event Data 3 [3:0] – Event Trigger Offset = 1h = State Asserted
15	Event Data 2	Not used
16	Event Data 3	Not used

11.5.1 BMC Watchdog Sensor – Next Steps

A SEL event is logged when either the BMC FW stack is reset or the BMC CPU itself is reset.

1. Check the SEL for any other events around the time of the failure.
2. Take note of all IPMI activity that was occurring around the time of the failure. Capture a System BMC Debug Log as soon as possible after the failure. This log can be captured from the Integrated BMC Web Console or by using the Intel Server Configuration Utility (`syscfg/sbmcdl Public filename.zip`). Send the log file to the system manufacturer or Intel representative for failure analysis.

11.6 BMC Firmware Health Sensor

The BMC tracks the health of each of its IPMI sensors and reports failures by providing a "BMC FW Health" sensor of the IPMI 2.0 sensor type Management Subsystem Health with support for the Sensor Failure offset. Only assertions are logged into the SEL for the Sensor Failure offset. The BMC Firmware Health sensor asserts for any sensor when ten consecutive sensor errors are read. These are not standard sensor events (that is, threshold crossings or discrete assertions). These are BMC Hardware Access Layer (HAL) errors such as I^2C NAKs or internal errors while attempting to read a register. If a successful sensor read is completed, the counter resets to zero.

Table 104. BMC firmware health sensor typical characteristics

Byte	Field	Description
11	Sensor Type	`28h` = Management Subsystem Health
12	Sensor Number	`10h`
13	Event Direction and Event Type	[7] Event direction `0b` = Assertion Event `1b` = Deassertion Event [6:0] Event Type = `6Fh` (Sensor Specific)
14	Event Data 1	[7:6] – `11b` = Sensor-specific event extension code in Event Data 2 [5:4] – `00b` = Unspecified Event Data 3 [3:0] – Event Trigger Offset = `4h` = Sensor failure
15	Event Data 2	Sensor number of the failed sensor
16	Event Data 3	Not used

11.6.1 BMC Firmware Health Sensor – Next Steps

1. Check the SEL for any other events around the time of the failure.
2. Take note of all IPMI activity that was occurring around the time of the failure. Capture a System BMC Debug Log as soon as possible after the failure. This log can be captured from the Integrated BMC Web Console or by using the Intel Server Configuration Utility (`syscfg/sbmcdl Public filename.zip`). Send the log file to the system manufacturer or Intel representative for failure analysis.
3. If the failure continues around a specific sensor, replace the board with that sensor.

11.7 Firmware Update Status Sensor

The BMC firmware supports a single Firmware Update Status sensor. This sensor is used to generate SEL events related to updates of embedded firmware on the platform. This includes updates to the BMC, BIOS, and Intel ME firmware.

This sensor is an event-only sensor that is not readable. Event generation is only enabled for assertion events.

Table 105. Firmware update status sensor typical characteristics

Byte	Field	Description
11	Sensor Type	2Bh (Version Change)
12	Sensor Number	12h
13	Event Direction and Event Type	[7] Event direction 0b = Assertion Event 1b = Deassertion Event [6:0] Event Type = 70h = OEM defined
14	Event Data 1	Event Trigger Offset 00h = Update started 01h = Update completed successfully 02h = Update failure
15	Event Data 2	[Bits 7:4] Target of update 0000b = BMC 0001b = BIOS 0010b = ME All other values are reserved. [Bits 3:1] Target instance (zero-based) [Bits 0:0] Reserved
16	Event Data 3	Not used

11.8 Add-in Module Presence Sensor

Some server boards provide dedicated slots for add-in modules/boards (for example, SAS, IO, and PCIe riser). For these boards, the BMC provides an individual presence sensor to indicate whether the module/board is installed.

Table 106. Add-in module presence sensor typical characteristics

Byte	Field	Description
11	Sensor Type	15h = Module/Board
12	Sensor Number	0Eh = IO Module Presence 0Fh = SAS Module Presence 13h = IO Module2 Presence
13	Event Direction and Event Type	[7] Event direction 0b = Assertion Event 1b = Deassertion Event [6:0] Event Type = 08h (“digital” discrete)
14	Event Data 1	[7:6] – 00b = Unspecified Event Data 2 [5:4] – 00b = Unspecified Event Data 3 [3:0] – Event Trigger Offset 0h = Device Removed / Device Absent 1h = Device Inserted / Device Present
15	Event Data 2	Not used
16	Event Data 3	Not used

11.8.1 Add-in Module Presence – Next Steps

If an unexpected device is removed or inserted, ensure that the module has been seated properly.

11.9 Intel® Xeon Phi™ Coprocessor Management Sensors

The Intel® Xeon® processor E5 4600/2600/2400/1600 product family BMC supports limited manageability of the Intel® Xeon Phi™ coprocessor adapter as described in this section. The Intel Xeon Phi coprocessor adapter uses the Many Integrated Core (GPGPU) architecture and the sensors are referred to as GPGPU sensors.

For each manageable Intel Xeon Phi coprocessor adapter found in the system, the BMC automatically enables the associated thermal margin sensors (0xC4-0xC7) and status sensors (0xA2, 0xA3, 0xA6, 0xA7).

11.9.1 Intel® Xeon Phi™ Coprocessor (GPGPU) Thermal Margin Sensors

The management controller firmware of the Intel Xeon Phi coprocessor adapter provides an IPMI sensor that is read to get the temperature data. The BMC then instantiates its own version of this sensor, which is used for fan speed control.

The thermal margin sensor is the difference between the Core Temp sensor value and the TControl value reported by the Intel Xeon Phi Coprocessor adapter.

This sensor does not log events into the SEL.

11.9.2 Intel® Xeon Phi™ Coprocessor (GPGPU) Status Sensors

Every time DC power is turned on, the BMC checks for Intel Xeon Phi coprocessor adapters installed in the system. All compatible cards are enabled for management. The status sensor is a direct copy of the status sensor reported by the Intel Xeon Phi coprocessor adapter.

Table 107. GPGPU status sensors typical characteristics

Byte	Field	Description
11	Sensor Type	C0h = OEM defined
12	Sensor Number	A2h = GPGPU 1 Status A3h = GPGPU 2 Status A6h = GPGPU 3 Status A7h = GPGPU 4 Status
13	Event Direction and Event Type	[7] Event direction 0b = Assertion Event 1b = Deassertion Event [6:0] Event Type = 70h (OEM defined)
14	Event Data 1	[7:6] – 00b = Unspecified Event Data 2 [5:4] – 00b = Unspecified Event Data 3 [3:0] – Event Trigger Offset Refer to the latest Intel® Xeon Phi™ coprocessor adapter specification.
15	Event Data 2	Not used
16	Event Data 3	Not used

11.9.2.1 Intel® Xeon Phi™ Coprocessor (GPGPU) Status Sensors Next Steps

Refer to the latest Intel Xeon Phi coprocessor adapter specification for the next steps.

11.10 Sensor Data Record (SDR) Auto-Config Fault

The BMC provides monitoring of the health status of the sensor data record (SDR) auto-configuration feature. The BMC firmware supports a discrete IPMI sensor for reporting and logging this fault condition.

The single supported sensor offset is asserted when both of the following are true:

- The BMC's SDR auto-configuration feature fails and
- The BMC's SDR auto-configuration feature is set to 'enabled'.

The offset is set to a deasserted state when either of the following is true:

- The BMC successfully completes an SDR auto-configuration cycle (resulting in auto-detecting the chassis and updating the SDR repository accordingly), regardless of the triggering event or
- The BMC's SDR auto-configuration feature is set to 'disable'.

Table 108. SDR auto-config fault sensor

Byte	Field	Description
11	Sensor Type	28h = Mgmt Health
12	Sensor Number	87h
13	Event Direction and Event Type	[7] Event direction 0b = Assertion Event 1b = Deassertion Event [6:0] Event Type = 03h ("digital" Discrete)
14	Event Data 1	[7:6] – 00b = Unspecified Event Data 2 [5:4] – 10b = OEM code in Event Data 3 [3:0] – Event Trigger Offset = 1h = State Asserted
15	Event Data 2	Not used
16	Event Data 3	[7:3] – reserved [2:0]: - OEM code for type of auto-config error 0h = CFG syntax error 1h = Chassis auto-detect error 2h = SDR/CFG file mismatch 3h = SDR or CFG file corrupted 4h = SDR syntax error All other values reserved

11.10.1 SDR Auto-Config Fault Sensor – Next Steps

1. Check update/upload SDR file and Config file correctly.
2. Check if FRU is valid.
3. Check cable connection especially PSU PMBus cable.

11.11 Invalid user name or password sensor

The BMC firmware supports a single Bad User Password sensor. This sensor is used to generate SEL events related to invalid user name or password attempts for BMC access with an IPMI message encapsulated in RMCP/RMCP+. SEL logging will follow the bad password threshold setting from the LAN parameters, and the end user can set/get the bad password threshold by set/getting the LAN configuration command.

Table 109. Bad User PWD sensor

Byte	Field	Description
11	Sensor Type	2Ah = Session Audit
12	Sensor Number	D7h
13	Event Direction and Event Type	[7] Event direction 0b = Assertion Event 1b = Deassertion Event [6:0] Event Type = 6Fh (Sensor Specific)
14	Event Data 1	[7:6] – 00b = Unspecified Event Data 2 [5:4] – 10b = OEM code in Event Data 3 [3:0] – Event Trigger Offset 02h - Invalid Username or Password 03h – Invalid password disable
15	Event Data 2	[7:6] Reserved [5:0] User ID 0x00 = unspecified
16	Event Data 3	[7:4] Reserved [3:0] Channel number

11.12 Remote debug sensor

To reduce the risk of an administrator unknowingly exposing the Remote PECI Debug as a potential attack point, the BMC supports an IPMI sensor to report the configuration state of Remote Debug features.

Table 110. Remote Debug Sensor

Byte	Field	Description
11	Sensor Type	DBh – OEM Defined.
12	Sensor Number	DBh
13	Event Direction and Event Type	[7] Event direction 0b = Assertion Event 1b = Deassertion Event [6:0] Event Type = 71h(OEM Defined)
14	Event Data 1	[7:6] – 00b = Unspecified Event Data 2 [5:4] – 10b = OEM code in Event Data 3 [3:0] – Event Trigger Offset 00h - Remote JTAG Consent 01h - Remote JTAG Enabled 02h - Remote JTAG Session 03h - Remote PECI Enabled 04h - Remote PECI Session
15	Event Data 2	[7:5] – Reserved [4] – PECI Enabled 0b: Disabled 1b: Enabled [3] – PECI Session State 0b: Idle

Byte	Field	Description
		1b: Session in progress [2] – JTAG Debug Consent 0b: Consent not given 1b: Consent given [1] – JTAG Enabled 0b: Disabled 1b: Enabled [0] – JTAG Session State 0b: Idle 1b: Session in progress
16	Event Data 3	[7:0] –FFh Unspecified.

11.13 System Firmware Security Sensor

The BMC supports a Firmware Security Sensor for logging a SEL event for security of BMC Firmware image authentication result in different phase.

Table 111. System Firmware Security Sensor

Byte	Field	Description
11	Sensor Type	C3h – OEM defined
12	Sensor Number	1Ah
13	Event Direction and Event Type	[7] Event direction 0b = Assertion Event 1b = Deassertion Event [6:0] Event Type = 7Bh(OEM Defined)
14	Event Data 1	[7:6] – 00b = Unspecified Event Data 2 [5:4] – 10b = OEM code in Event Data 3 [3:0] – Event Trigger Offset 00h Authentication Failure of BMC Firmware Image During Boot 01h Invalid Security Revision of BMC Firmware Image During Boot 02h Authentication Failure of BMC Firmware Image During Update 03h Invalid Security Revision of BMC Firmware Image During Update 04h Authentication Failure of Signed Region During Update 05h Authentication Failure of Signed Region During Boot or Runtime 06h Invalid Security Revision of Signed Region During Update 07h Invalid Security Revision of Signed Region During Boot or Runtime 0Ch Factory Image Booted 0Dh Factory Security Revision Downgraded
15	Event Data 2	[7:0] - Image Type
16	Event Data 3	[7:0] –FFh Unspecified.

11.14 KCS Policy Sensor

KCS (Keyboard Controller Style) interface is the single-wire bus which directly connecting the BMC and the host CPU. Host software including operating system, applications, and BIOS access the BMC through KCS. There is no authentication established for KCS. Communication through this bus is in plain raw data without any authentication and authorization needed. Through KCS, host software can perform operations, which should be in highest privilege. This exposes security risks, as any compromised operating system will allow a potential hacker to gain control of the BMC.

To mitigate the security risk, the BMC firmware implements KCS Policy Control Modes to allow an authenticated BMC administrative user to control the level of protection from IPMI commands executed over the KCS channels. Within this generation of BMC firmware, 3 different KCS Policy Control Modes are supported:

KCS Policy Control Mode – Allow All

This configuration setting is intended for normal IPMI compliant communications between the Host operating system and the BMC. This mode should be used when provisioning the BMC configuration for deployment.

KCS Policy Control Mode – Deny All

This configuration setting disables the IPMI KCS command interfaces between the Host operating system and the BMC. This is a non-compliant IPMI configuration that will impact the operation of the server management software running on the Host operating system. This only applies to the IPMI commands over the KCS interfaces, and does not apply to the authenticated network interfaces to the BMC.

KCS Policy Control Mode – Restricted

This configuration setting enables the use of an Access Control List by the BMC Firmware that allows applications executing on the host operating system to have access to a limited set of IPMI commands using the KCS interfaces. This is a non-compliant IPMI configuration that may impact the operation of the server management software running on the Host operating system. For example, the IPMI commands that are used to provision the BMC configuration settings, or control the state of the Host operating system, will be disallowed when the BMC KCS interface is in restricted mode. This only applies to the IPMI commands over the KCS interfaces, and does not apply to the authenticated network interfaces to the BMC.

KCS access is required for the host BIOS during Pre-Boot phase. BIOS communicates with BMC for platform configurations through these channels. Thus BIOS use of KCS is trusted between a platform reset and the end of the BIOS DXE phase. For unconditional and conditional KCS access, two host phases are needed:

1. Pre-Boot phase. This is the phase between platform reset and the end of DXE signaled by the CORE-BIOS-DONE signal before option ROMs are executed. BMC has the below assumptions and KCS handling policies:
   - Core BIOS is trusted
   - KCS commands accepted from BIOS without authentication
   - Transitions to Post-Boot after BIOS sends CORE-BIOS-DONE signal to BMC
2. Post-Boot phase. This is the phase for BIOS to load option ROMs, boot the host operating system, and perform host operating system execution. BMC assumptions and KCS handling policies are as below:
   - Triggered by CORE-BIOS-DONE signal from BIOS
   - When KCS Policy Control Mode is set to “Allow All”

  - KCS commands accepted from BIOS/EFI, Host operating system (Ring0) without authentication
  - Warning Indicator set (EWS banner with explanatory help text, security sensor)
  - Transitions to “Restricted” or “Deny All” with IPMI command from any interface
- When KCS Policy Control Mode is set to “Restricted” or “Deny All”:
  - Triggered by IPMI Command to set KCS Policy Control Mode out of “Allow All”
  - In KCS Restricted Mode, only KCS commands listed in the Access Control List (ACL) are accepted from BIOS/EFI, Host operating system (Ring 0) without authentication, or no KCS commands in “Deny All” Mode.
  - May transition back to KCS “Allow All” Mode with:
    - Authenticated IPMI/RMCP+ command from OOB (LAN etc.)
    - Authenticated EWS/Redfish operations
    - Force Firmware Update Jumper (safe mode) allows reset mode from KCS

The following table shows under each KCS Policy Control Mode and host booting phase, KCS commands will be serviced or not.

Table 112. BMC KCS Policy Control Modes and KCS command service definition

KCS Policy Control Modes	Description	Pre-Boot	Post-Boot
Allow All	• Default state when customer receives board • Alerts on EWS page and/or security sensor warn owner that the BMC is an unsafe state • Can re-enter KCS Policy Control Mode “Allow All” through authenticated OOB interface or through FFUJ (KCS allowed in safe mode)	All KCS Commands Permitted	All KCS Commands Permitted
Restricted	• Transitions from “Allow All” when platform owner issues command to set KCS Policy Control Mode (or EWS)	All KCS Commands Permitted	Only commands in the Access Control List are permitted
Deny All	• Transitions from other modes when platform owner issues commands to set KCS Policy Control Mode (EWS).	All KCS Commands Permitted	No KCS Commands Permitted

BMC implements OEM type sensor with offsets set to 3 KCS Policy Control Mode. SEL will be captured if KCS Policy Control Mode is changed.

Table 113. KCS Policy Sensor

Byte	Field	Description
11	Sensor Type	DAh – KCS Mode
12	Sensor Number	DAh
13	Event Direction and Event Type	[7] Event direction 0b = Assertion Event 1b = Deassertion Event [6:0] Event Type = 7Ah(OEM Defined)
14	Event Data 1	[7:6] – 00b = Unspecified Event Data 2 [5:4] – 00b = Unspecified Event Data 3 [3:0] – Event Trigger Offset 03h = KCS Allow all Mode 04h = KCS Restricted mode 05h = KCS Deny all mode
15	Event Data 2	[7:0] – FFh Unspecified.
16	Event Data 3	[7:0] – FFh Unspecified.

11.15 OOB Firmware update Sensor

OOB (Out of Band) supports a firmware update feature in addition with BIOS configuration. In this while BIOS is booting, BIOS queries BMC for the availability of firmware for update (BIOS/FD/ME Capsule files). If the files are available, then BIOS fetches and detects the files from BMC and update the same. After the successful update process, the BIOS triggers a reset. The changes related to the update are expected to be reflected after this reset. BIOS will send a SEL to BMC after OOB Firmware update.

Table 114. OOB Firmware update sensor typical characteristics

Byte	Field	Description
11	Sensor Type	12h - System Event
12	Sensor Number	83h
13	Event Direction and Event Type	[7] Event direction 0b = Assertion Event 1b = Deassertion Event [6:0] Event Type = 6Fh(Sensor-Specific)
14	Event Data 1	[7:6] – 11b = Unspecified Event Data 2 [5:4] – 11b = Unspecified Event Data 3 [3:0] – Event Trigger Offset 9h = USB Mount Failed Ah = Virtual USB File Read Failed Bh = Password Check Passed Ch = Password Check Failed Dh = Invalid Capsule
15	Event Data 2	ED2 = [7:0] = Image Type(Only valid when Offset Value is Dh) 2 = BIOS Image 3 = ME Image 4 = FD Image
16	Event Data 3	ED3 = [7:0] = OOB Operation 0 = OOB Update

11.16 OOB BIOS Configuration Sensor

OOB (Out of Band) BIOS configuration provides the ability for the user to view and modify the BIOS setup configuration parameters remotely via BMC LAN channel at any Host state or in an operating system booted (running) state. Modifications to the parameters take place upon the next system reboot. A SEL will send to BMC after using this function.

Table 115. OOB BIOS Configuration sensor typical characteristics

Byte	Field	Description
11	Sensor Type	12h - System Event
12	Sensor Number	83h
13	Event Direction and Event Type	[7] Event direction 0b = Assertion Event 1b = Deassertion Event [6:0] Event Type = 6Fh(Sensor-Specific)
14	Event Data 1	[7:6] – 11b = Unspecified Event Data 2 [5:4] – 11b = Unspecified Event Data 3 [3:0] – Event Trigger Offset 9h = XML Update Passed Ah = XML Update Failed Bh = Password Check Passed Ch = Password Check Failed
15	Event Data 2	ED2 = [7:0] = Image Type 0 = XML Type 0 1 = XML Type 1
16	Event Data 3	ED3 = [7:0] = OOB Operation 1 = OOB BIOS Config

12. Hot-Swap Controller Backplane Events

In all Intel® Server Systems based on Intel® Xeon® processor E5 4600/2600/2400/1600 product families, Intel® Server Board based on Intel® Xeon® Scalable processor family and Intel® Server Board based on 2nd Gen Intel® Xeon® Scalable processor family, Intel® Server Board based on Intel® Xeon® Platinum 9200 Processor Family, the backplanes follow a hybrid architecture, in which the IPMI functionality previously supported in the hot-swap controller (HSC) is integrated into the BMC family.

12.1 Hot-Swap Controller (HSC) Backplane Temperature Sensor

There is a thermal sensor on the Hot-Swap Backplane to measure the ambient temperature.

Table 116. HSC backplane temperature sensor typical characteristics

Byte	Field	Description
11	Sensor Type	01h = Temperature
12	Sensor Number	29h = HSBP 1 Temp 2Ah = HSBP 2 Temp 2Bh = HSBP 3 Temp E0h = HSBP 4 Temp
13	Event Direction and Event Type	[7] Event direction 0b = Assertion Event 1b = Deassertion Event [6:0] Event Type = 01h (Threshold)
14	Event Data 1	[7:6] – 01b = Trigger reading in Event Data 2 [5:4] – 01b = Trigger threshold in Event Data 3 [3:0] – Event Trigger Offset as described in Table 117
15	Event Data 2	Reading that triggered event
16	Event Data 3	Threshold value that triggered event

Table 117. HSC backplane temperature sensor – event trigger offset – next steps

Event Trigger		Assertion Severity	Deassertion Severity	Description	Next Steps
00h	Lower non-critical going low	Degraded	OK	The temperature has dropped below its lower non-critical threshold.	1. Check for clear and unobstructed airflow into and out of the chassis. 2. Ensure the SDR is programmed and correct chassis has been selected. 3. Ensure there are no fan failures. 4. Ensure the air used to cool the system is within the thermal specifications for the system (typically below 35 °C).
02h	Lower critical going low	Non-fatal	Degraded	The temperature has dropped below its lower critical threshold.	
07h	Upper non-critical going high	Degraded	OK	The temperature has gone over its upper non-critical threshold.	
09h	Upper critical going high	Non-fatal	Degraded	The temperature has gone over its upper critical threshold.	

12.2 Hard Disk Drive Monitoring Sensor

The new backplane design for Intel® Server Systems based on Intel® Xeon® processor E5 4600/2600/2400/1600 product families, Intel® Server Board based on Intel® Xeon® Scalable processor family and Intel® Server Board based on 2nd Gen Intel® Xeon® Scalable processor family, moves IPMI ownership of the HDD sensors to the BMC. Systems may have multiple storage backplanes. Hard Disk Drive status monitoring is supported through disk status sensors owned by the BMC.

Table 118. Hard disk drive monitoring sensor typical characteristics

Byte	Field	Description
11	Sensor Type	0Dh = Drive Slot (Bay)
12	Sensor Number	60h-68h = Hard Disk Drive 15–23 Status E2h-E3h = Rear Hard Disk Drive 0–1 Status F0h-FEh = Hard Disk Drive 0–14 Status
13	Event Direction and Event Type	[7] Event direction 0b = Assertion Event 1b = Deassertion Event [6:0] Event Type = 6Fh (Sensor Specific)
14	Event Data 1	[7:6] – 00b = Unspecified Event Data 2 [5:4] – 00b = Unspecified Event Data 3 [3:0] – Event Trigger Offset as described in Table 119
15	Event Data 2	Not used
16	Event Data 3	Not used

Table 119. Hard disk drive monitoring sensor – event trigger offset – next steps

Event Trigger	Description	Next Steps
00h	Drive Presence	If during normal operation the state changes unexpectedly, ensure that the drive is seated properly and the drive carrier is properly latched. If that does not work, replace the drive.
01h	Drive Fault	
07h	Rebuild/Remap in progress	• This is expected after replacing a hard drive. • This is expected if the system has a hot spare and one of the drives failed. Check logs for which drive has failed. • If this is seen unexpectedly, it could be an indication of a drive that is close to failing.

12.3 Hot-Swap Controller Health Sensor

The BMC supports an IPMI sensor to indicate the health of the Hot-Swap Controller (HSC). This sensor indicates that the controller is offline for the cases that the BMC either cannot communicate with it or it is stuck in a degraded state so that the BMC cannot restore it to full operation through a firmware update.

Table 120. HSC health sensor typical characteristics

Byte	Field	Description
11	Sensor Type	16h = Microcontroller
12	Sensor Number	69h = Hot-Swap Controller 1 Status 6Ah = Hot-Swap Controller 2 Status 6Bh = Hot-Swap Controller 3 Status
13	Event Direction and Event Type	[7] Event direction 0b = Assertion Event 1b = Deassertion Event [6:0] Event Type = 0Ah (Discrete)
14	Event Data 1	[7:6] – 00b = Unspecified Event Data 2 [5:4] – 00b = Unspecified Event Data 3

Byte	Field	Description
		[3:0] – Event Trigger Offset = 4h = Transition to offline
15	Event Data 2	Not used
16	Event Data 3	Not used

12.3.1 HSC Health Sensor – Next Steps

1. Ensure that all connections to the HSC are well seated.
2. Cross test with another HSC. If the issue remains with the HSC, replace the HSC, otherwise start cross testing all interconnections.

13. Intel® Management Engine (Intel® ME) Events

The Intel® Management Engine (Intel® ME) controls the platform environmental control interface (PECI) and also contains the Intel® Node Manager (Intel® NM) functionality.

13.1 Intel® ME Firmware Health Event

This sensor is used in Platform Event messages to the BMC containing health information including but not limited to firmware upgrade and application errors.

Table 121. Intel® ME firmware health event sensor typical characteristics

Byte	Field	Description
8, 9	Generator ID	002Ch or 602Ch – Intel ME Firmware
11	Sensor Type	DCh = OEM
12	Sensor Number	17h
13	Event Direction and Event Type	[7] Event direction 0b = Assertion Event 1b = Deassertion Event [6:0] Event Type = 75h (OEM)
14	Event Data 1	[7:6] – 10b = OEM code in Event Data 2 [5:4] – 10b = OEM code in Event Data 3 [3:0] – Health event type – 0h (Firmware Status) – 1h (SMBus link failure)
15	Event Data 2	See Table 122
16	Event Data 3	See Table 122

13.1.1 Intel® ME Firmware Health Event – Next Steps

In Table 122, Event Data 3 is only noted for specific errors.

If the issue continues to be persistent, provide the content of Event Data 3 to Intel support team for interpretation. Event Data 3 codes are in general not documented, because their meaning only provides some clues, varies, and usually needs to be individually interpreted.

Table 122. Intel® ME firmware health event sensor – next steps

ED1	ED2	Description	ED3	Description	Next Steps
00h	00h	Recovery GPIO forced. Recovery Image loaded due to recovery MGPIO pin asserted. Pin number is configurable in factory presets. Default recovery pin is MGPIO1.			Deassert MGPIO1 and reset the Intel® ME.
	01h	Image execution failed. Recovery Image or backup operational image loaded because operational image is corrupted. This may be either caused by flash device			Either the flash device must be replaced (if error is persistent) or the upgrade procedure must be started again.

ED1	ED2	Description	ED3	Description	Next Steps
		corruption or failed upgrade procedure.			
	02h	Flash erase error. Error during Flash erasure procedure probably due to Flash part corruption.			The flash device must be replaced.
	03h	Flash state information.	00h	Flash partition table, recovery image, or factory presets image corrupted.	Check extended information byte in Event Data 3 (byte 7) whether this is wear-out protection causing this event. If so wait until wear-out protection expires, otherwise probably the flash device must be replaced (if error is persistent).
			01h	Flash erase limit has been reached.	
			02h	Flash write limit has been reached; writing to flash has been disabled.	
			03h	Writing to the flash has been enabled.	
	04h	Internal error. Error during firmware execution – FW Watchdog Timeout.			Firmware should automatically recover from error state. If error is persistent, then operational image should be updated or hardware board repair is needed.
	05h	BMC did not respond correctly to Chassis Control - Power Down command triggered by Intel Node Manager policy failure action and Intel® ME forced shutdown.			Verify the Intel® Node Manager policy configuration.
	06h	Direct Flash update requested by the BIOS. Intel® ME firmware will switch to recovery mode to perform full update from the BIOS.			This is transient state. Intel® ME firmware will return to operational mode after successful image update performed by the BIOS.
	07h	Manufacturing error. Wrong manufacturing configuration detected by Intel® ME firmware.	00h	Generic error.	If error is persistent the Flash device must be replaced or FW configuration must be updated.
			01h	Wrong or missing VSCC table.	
			02h	Wrong sensor scanning period in PIA.	
			03h	Wrong device definition in PIA.	
			04h	Reserved (Wrong SMART/CLST configuration).	
			05h	Intel® ME FW configuration is inconsistent or out of range.	
			06h	Reserved.	
			07h	Intel® ME FW configuration is corrupted.	
			08h	SMLink0/0B misconfiguration.	
	08h	Automatic Restore to Factory Presets.	00h	Flash file system error detected. Automatic restore to factory presets has been triggered.	If error is persistent the Flash device must be replaced.

ED1	ED2	Description	ED3	Description	Next Steps
			01h	Automatic restore to factory presets has been completed.	
			02h	Restore to factory presets triggered by “Force ME Recovery” IPMI command has been completed.	
			03h	Restore to factory presets triggered by AC power cycle with Recovery jumper asserted has been completed.	
	09h	Firmware Exception.			Restore factory presets using “Force ME Recovery” IPMI command or by doing AC power cycle with Recovery jumper asserted. If this does not clear the issue, reflash the SPI flash. If the issue persists, provide the content of Event Data 3 to Intel support team for interpretation. (Event Data 3 codes are not documented because they only provide clues that must be interpreted individually).
	0Ah	Flash Wear-Out Protection Warning. Warning threshold for number of flash operations has been exceeded.		Percentage of flash write operations, which have been conducted.	No immediate repair action needed. This is just a warning event.
	0Dh	PECI over DMI interface error. This is a notification that PECI over DMI interface failure was detected and it is not functional anymore. It may indicate the situation when PECI over DMI was not configured by BIOS or a defect, which may require a CPU Host reset to recover from.	01h	DRAM Init Done HECI message not received by Intel® ME before EOP.	Recovery via CPU Host reset or platform reset.
			02h	System PCIe* bus configuration not known or not valid on DID HECI message arrival to Intel® ME.	
			03h	PECI over DMI run-time failure.	
	0Eh	MCTP interface error. This is a notification that MCTP interface failure was detected and it is not functional anymore. It may indicate the situation when MCTP was not configured by BIOS or a defect, which may need a Host reset to recover from.	01h	No DID HECI message received before EOP.	Recovery via CPU Host reset or platform reset.
			02h	No MCTP_SET_BUS_OWNER HECI message received by Intel® ME on EOP arrival to ME, while MCTP stack is configured in Bus Owner Proxy mode.	
	0Fh	Auto-configuration finished. Operational image finished power source auto-configuration.		[7] – Auto-configuration result 0b – Success 1b – Failure if bit 7 reports Success (0b) then the other bits are defined as follows;	Auto-configuration could be enforced by restore to factory defaults.

ED1	ED2	Description	ED3	Description	Next Steps
				[6:5] – DC Power source 00b – BMC 01b – PSU 10b – On-board power sensor 11b – reserved [4:3] – Chassis Power input source 00b – BMC 01b – PSU 10b – On-board power sensor/ PSU efficiency 11b – not supported [2:1] – PSU efficiency source 00b – BMC 01b – PSU 10b – reserved 11b – not supported [0] – Unmanaged power source 0b – BMC 1b – estimated if bit [7] reports failure (1b) then the other bits are defined as follows; [6:5] – Failure 00b – BMC discovery failure 01b – Insufficient factory configuration 10b – Unknown sensor type 11b – Other error encountered [4:0] – Reserved For Event Data 2 (byte 6) equal to 10h 00h – Other Segment Defined Feature 01h – Fast NM limiting 02h – Volumetric Airflow and Outlet Temperature 03h – CUPS 04h – Thermal policies and Inlet Temperature 05h – Platform limiting with MICs 07h – Shared power supplies 08h – MIC Proxy 09h – Reset warning 0Ah – PMBus Proxy 0Bh – Always on 0Ch – IPMI Intel® ME FW update 0Dh – MCTP bus owner 0Eh – MCTP bus owner proxy 0Fh – Dual BIOS 10h – Battery less	
	10h	Unsupported Segment Defined Feature. Feature not supported in current segment detected by Intel® ME Firmware.			Proper FW configuration must be updated or use the Flash device with proper FW configuration.
	11h	Reserved.			
	12h	CPU Debug Capability Disabled.			

ED1	ED2	Description	ED3	Description	Next Steps
	13h	UMA operation error. This is a notification that UMA was not initialized correctly during POST or error occurred while copying page to/from UMA. It may indicate situations when BIOS did not grant memory for UMA, granted memory size differs from requested, checksum of copied page differs from expected or timeout occurred during copying data to/from UMA.	00h	UMA Read integrity error. Checksum of data read from UMA differs from expected one.	Platform reset when UMA not configured correctly, or when error occurred during normal operation on correctly configured UMA multiple times leading to Intel® ME entering Recovery or restricted operation mode.
			01h	UMA Read/Write timeout. Timeout occurred during copying data from/to UMA.	
			02h	UMA not granted. BIOS did not grant any UMA or DRAM INIT done message was not received from BIOS before EOP. Intel® ME FW goes to recovery.	
			03h	UMA size granted by BIOS differs from requested. ME FW goes to recovery.	
	14h – 15h	Reserved.			
	16h	Intel PTT Health Event.	00h	Intel PTT disabled (PTT region is not present).	
			01h	Intel PTT downgrade (PTT data should be not available).	
			02h	Intel PTT disabled (battery less configuration).	
	17h	Boot Guard Health Event.	00h	Boot Guard flow error (verification timeout, verification error or BIOS Protection error). For event data 2 (byte 6) equal to 18h	
			01h	Firmware entered restricted mode – UMA is not available, restricted features set.	
			02h	Firmware exited restricted mode.	
	18h	Restricted mode information. Firmware entered restricted mode due to error conditions met, or exited restricted mode due to Intel® ME reset or entering recovery mode.			
	19h	MultiPCH mode misconfiguration.	01h	BIOS did not set reset synchronization in multiPCH mode.	
			02h	PMC indicates different non/legacy mode for the PCH than BMC set on the GPIO.	
			03h	Misconfiguration MPCH support enabled due to BTG support enabled.	
	1Ah		00h	OEM Public Key verification error.	

ED1	ED2	Description	ED3	Description	Next Steps
		Flash Descriptor Region Verification Error.	01h	Flash Descriptor Region Manifest verification error.	Flash Descriptor Region must be created correctly.
			02h	Soft Straps verification error.	
	1Bh – FFh	Reserved.			
01h	01h	error was detected on SMLINK0/SMLINK0B.		MUX address if there is a problem with a bus segment behind a MUX or FFh if there is a problem with the whole SMBus link. The address field format depends on the MUX type. For MGPIO MUX; [0:5] = Mux MGPIO index. [6:7] = Reserved, set to 00b. For SMBus MUX; [0] – Reserved, set to 0b. [7:1] – 7-bit SMBus MUX address.	
	02h	error was detected on SMLINK1.			
	03h	error was detected on SMLINK2.			
	04h	error was detected on SMLINK3.			
	05h	error was detected on SMLINK4.			

13.2 Intel® Node Manager Exception Event

An Intel Node Manager exception event is sent each time maintained policy power limit is exceeded over Correction Time Limit.

Table 123. Intel Node Manager exception sensor typical characteristics

Byte	Field	Description
8, 9	Generator ID	002Ch or 602Ch – Intel ME Firmware
11	Sensor Type	DCh = OEM
12	Sensor Number	18h
13	Event Direction and Event Type	[7] Event direction 0b = Assertion Event 1b = Deassertion Event [6:0] Event Type = 72h (OEM)
14	Event Data 1	[7:6] – 10b = OEM code in Event Data 2 [5:4] – 10b = OEM code in Event Data 3 [3] – Node Manager Policy event 0 – Reserved 1 – Policy Correction Time Exceeded – Policy did not meet the contract for the defined policy. The policy continues to limit the power or shut down the platform based on the defined policy action. [2] – Reserved [1:0] – 00b
15	Event Data 2	[4:7] – Reserved [0:3] – Domain Id 00h – Entire platform. 01h – CPU subsystem. 02h – Memory subsystem. 03h – HW Protection. 04h – High Power I/O subsystem. Others – Reserved
16	Event Data 3	Policy Id

13.2.1 Intel Node Manager Exception Event – Next Steps

This is an informational event. Next steps depend on the policy that was set. See the *Intel Node Manager Specification* for more details.

13.3 Intel® Node Manager Health Event

An Intel Node Manager Health Event message provides a runtime error indication about Intel® Intelligent Power Node Manager's health. Types of service that can send an error are defined as follows:

- Misconfigured policy Error reading power data.
- Error reading inlet temperature.

Table 124. Intel Node Manager health event sensor typical characteristics

Byte	Field	Description
8, 9	Generator ID	002Ch or 602Ch – Intel ME Firmware
11	Sensor Type	DCh = OEM
12	Sensor Number	19h
13	Event Direction and Event Type	[7] Event direction 0b = Assertion Event 1b = Deassertion Event [6:0] Event Type = 73h (OEM)
14	Event Data 1	[7:6] – 10b = OEM code in Event Data 2 [5:4] – 10b = OEM code in Event Data 3 [3:0] – Health Event Type = 02h (Sensor Node Manager)
15	Event Data 2	[7:4] – Error type 0–7 – Reserved 8 – Outlet Temperature Reading Failure 9 – Volumetric Airflow Reading Failure 10 – Policy Misconfiguration 11 – Power Sensor Reading Failure 12 – Inlet Temperature Reading Failure 13 – Host Communication error 14 – Real-time clock synchronization failure 15 – Platform shutdown initiated by NM policy due to execution of action defined by Policy Exception Action [3:0] – Domain Id 00h – Entire platform 01h – CPU subsystem 02h – Memory subsystem 03h – HW Protection 04h – High Power I/O subsystem Others – Reserved
16	Event Data 3	If Error type = 10 or 15 <Policy Id> If Error type = 11 <Power Sensor Address> If Error type = 12 <Inlet Sensor Address> Otherwise set to 0.

13.3.1 Intel® Node Manager Health Event – Next Steps

Misconfigured policy can happen if the max/min power consumption of the platform exceeds the values in policy due to hardware reconfiguration.

First occurrence of not acknowledged event will be retransmitted no faster than every 300 milliseconds.

Real-time clock synchronization failure alert is sent when Intel NM is enabled and capable of limiting power, but within 10 minutes the firmware cannot obtain valid calendar time from the host side, so Intel NM cannot handle suspend periods.

Next steps depend on the policy that was set. See the *Intel Node Manager Specification* for more details.

13.4 Intel® Node Manager Operational Capabilities Change

This message provides a runtime error indication about Intel Intelligent Power Node Manager's operational capabilities. This applies to all domains.

Assertion and deassertion of these events are supported.

Table 125. Intel® Node Manager operational capabilities change sensor typical characteristics

Byte	Field	Description
8, 9	Generator ID	002Ch or 602Ch – Intel ME Firmware
11	Sensor Type	DCh = OEM
12	Sensor Number	1Ah
13	Event Direction and Event Type	[7] Event direction 0b = Assertion Event 1b = Deassertion Event [6:0] Event Type = 74h (OEM)
14	Event Data 1	[7:6] – 00b = Unspecified Event Data 2 [5:4] – 00b = Unspecified Event Data 3 [3:0] – Current state of Operational Capabilities. Bit pattern: 0 – Policy interface capability 0 – Not Available 1 – Available 1 – Monitoring capability 0 – Not Available 1 – Available 2 – Power limiting capability 0 – Not Available 1 – Available
15	Event Data 2	Not used
16	Event Data 3	Not used

13.4.1 Intel® Node Manager Operational Capabilities Change – Next Steps

Policy Interface available indicates that Intel Intelligent Power Node Manager is able to respond to the external interface about querying and setting Intel Intelligent Power Node Manager policies. This is generally available as soon as the microcontroller is initialized.

Monitoring Interface available indicates that Intel Intelligent Power Node Manager can monitor power and temperature. This is generally available when firmware is operational.

Power limiting interface available indicates that Intel Intelligent Power Node Manager can do power limiting and is indicative of an Advanced Configuration and Power Interface (ACPI)-compliant operating system loaded (unless the OEM has indicated support for non-ACPI compliant operating system).

Current value of not acknowledged capability sensor is retransmitted no faster than every 300 milliseconds.

Next steps depend on the policy that was set. See the *Intel Node Manager Specification* for more details.

13.5 Intel® Node Manager Alert Threshold Exceeded

Policy Correction Time Exceeded Event is sent each time maintained policy power limit is exceeded over Correction Time Limit.

Table 126. Intel® Node Manager alert threshold exceeded sensor typical characteristics

Byte	Field	Description
8, 9	Generator ID	002Ch or 602Ch – Intel ME Firmware
11	Sensor Type	DCh = OEM
12	Sensor Number	1Bh
13	Event Direction and Event Type	[7] Event direction 0b = Assertion Event 1b = Deassertion Event [6:0] Event Type = 72h (OEM)
14	Event Data 1	[7:6] – 10b = OEM code in Event Data 2 [5:4] – 10b = OEM code in Event Data 3 [3] = Node Manager Policy event 0 – Threshold exceeded 1 – Policy Correction Time Exceeded – Policy did not meet the contract for the defined policy. The policy continues to limit the power or shut down the platform based on the defined policy action. [2] – Reserved [1:0] – Threshold Number. 0–2 – Threshold index
15	Event Data 2	[7:4] – Reserved [3:0] – Domain ID 00h – Entire platform 01h – CPU subsystem 02h – Memory subsystem 03h – HW Protection 04h – High Power I/O subsystem Others – Reserved
16	Event Data 3	Policy ID

13.5.1 Intel® Node Manager Alert Threshold Exceeded – Next Steps

First occurrence of not acknowledged event will be retransmitted no faster than every 300 milliseconds.

First occurrence of Threshold exceeded event assertion/deassertion will be retransmitted no faster than every 300 milliseconds.

Next steps depend on the policy that was set. See the *Node Manager Specification* for more details.

13.6 Intel® Node Manager SmaRT and CLST Sensor

The Intel Node Manager monitors the power supplies in the system for an SMBALERT# assertion in the power supplies. If it deems that this is caused by what would be considered a system SmaRT/CLST event, then it throttles the total system power to prevent the system failure. This is logged as a SmaRT/CLST event.

Table 127. Intel® Node Manager SmaRT/CLST event typical characteristics

Byte	Field	Description
8, 9	Generator ID	002Ch or 602Ch – Intel ME Firmware
11	Sensor Type	DCh = OEM
12	Sensor Number	B2h
13	Event Direction and Event Type	[7] Event direction 0b = Assertion Event 1b = Deassertion Event [6:0] Event Type = 03h (Digital Discrete)
14	Event Data 1	[7:6] – 01b = Previous state and/or severity in Event Data 2 [5:4] – 10b = OEM code in Event Data 3 [3:0] – Offset from Event/Reading Code 0h – State Deasserted 1h – State Asserted
15	Event Data 2	[7:4] – Optional offset from 'Severity' Event/Reading Code. 00h - transition to OK 01h - transition to noncritical from OK 02h - transition to critical from less severe 03h - transition to unrecoverable from less severe 04h - transition to noncritical from more severe 05h - transition to critical from unrecoverable 06h - transition to unrecoverable 07h - monitor 08h - informational [3:0] - Fh
16	Event Data 3	Corresponding Power Supply Status sensor number or 0 if the source of SmaRT and CLST assertion is external (for example BMC).

Table 128. SmaRT and CLST sensor severity codes

Severity Code	Description	PSU Condition
00h	Transition to OK	All present PSU faults disappeared.
01h	Transition to noncritical from OK	SMBAlert# has been asserted by PSU but it should be ignored (for example, PSU goes to off state due insufficient input voltage)
02h	Transition to critical from less severe	SMBAlert# was asserted due to one of the following PSU events: • UV_Fault or • OT_Warning or • OC_Warning
04h	Transition to noncritical from more severe	There has been a critical condition and one of the following events happened: • UV Fault lasted more than preconfigured time (default 500ms) or • PSU causing disappeared or • PSU unit become off or • OT warning lasted more than 500ms for one PSU and there is another PSU present with no OT warning.

13.6.1 Intel® Node Manager SmaRT/CLST Event – Next Steps

1. Look for any other events in the System Event Log for correlation.
2. Ensure that there are no issues with any of the installed power supplies.
3. If there is only one power supply, then consider adding an additional power supply to handle the required load.

14. Microsoft Windows* Records

With Microsoft Windows Server* 2003 R2 and later versions, an Intelligent Platform Management Interface (IPMI) driver was added. This added the capability of logging some operating system events to the SEL. The driver can write multiple records to the SEL for the following events:

- Boot
- Shutdown
- Bug Check / Blue Screen

14.1 Boot Event Records

When the system boots into the Microsoft Windows* operating system, two events can be logged. The first is a boot record and the second is an OEM event. These are informational only records.

Table 129. Boot event record typical characteristics

Byte	Field	Description
8, 9	Generator ID	0041h – System Software with an ID = 20h
11	Sensor Type	1Fh = Operating system Boot
12	Sensor Number	00h
13	Event Direction and Event Type	[7] Event direction 0b = Assertion Event 1b = Deassertion Event [6:0] Event Type = 6Fh (Sensor Specific)
14	Event Data 1	[7:6] – 00b = Unspecified Event Data 2 [5:4] – 00b = Unspecified Event Data 3 [3:0] – Event Trigger Offset = 1h = C: boot completed
15	Event Data 2	Not used
16	Event Data 3	Not used

Table 130. Boot OEM event record typical characteristics

Byte	Field	Description
1, 2	Record ID	ID used for SEL Record access.
3	Record Type	[7:0] – DCh = OEM timestamped, bytes 8–16 OEM defined.
4–7	Timestamp	Time when the event was logged. The least significant byte is first.
8–10	IPMI Manufacturer ID	0137h (311d) = IANA enterprise number for Microsoft.
11	Record ID	Sequential number reflecting the order in which the records are read. The numbers start at one for the first entry in the SEL and continue sequentially to *n*, the number of entries in the SEL.
12–15	Boot Time	Timestamp of when the system booted into the operating system.
16	Reserved	00h

14.2 Shutdown Event Records

When the system shuts down from the Microsoft Windows* operating system, multiple events can be logged. The first is an operating system Stop/Shutdown Event Record; this can be followed by a shutdown reason code OEM record, and then zero or more shutdown comment OEM records. These are all informational only records.

Table 131. Shutdown reason code event record typical characteristics

Byte	Field	Description
8, 9	Generator ID	0041h – System Software with an ID = 20h
11	Sensor Type	20h = Operating system Stop/Shutdown
12	Sensor Number	00h
13	Event Direction and Event Type	[7] Event direction 0b = Assertion Event 1b = Deassertion Event [6:0] Event Type = 6Fh (Sensor Specific)
14	Event Data 1	[7:6] – 00b = Unspecified Event Data 2 [5:4] – 00b = Unspecified Event Data 3 [3:0] – Event Trigger Offset = 3h = Operating system Graceful Shutdown
15	Event Data 2	Not used
16	Event Data 3	Not used

Table 132. Shutdown reason OEM event record typical characteristics

Byte	Field	Description
1, 2	Record ID	ID used for SEL Record access
3	Record Type	[7:0] – DDh = OEM timestamped, bytes 8–16 OEM defined
4–7	Timestamp	Time when the event was logged. LS byte first.
8–10	IPMI Manufacturer ID	0137h (311d) = IANA enterprise number for Microsoft
11	Record ID	Sequential number reflecting the order in which the records are read. The numbers start at one for the first entry in the SEL and continue sequentially to *n*, the number of entries in the SEL.
12–15	Shutdown Reason	Shutdown Reason code from the registry (LSB first): HKLM/Software/Microsoft/Windows/CurrentVersion/Reliability/shutdown/ReasonCode
16	Reserved	00h

Table 133. Shutdown comment OEM event record typical characteristics

Byte	Field	Description
1, 2	Record ID	ID used for SEL Record access
3	Record Type	[7:0] – DDh = OEM timestamped, bytes 8–16 OEM defined
4–7	Timestamp	Time when the event was logged. The least significant byte is first.
8–10	IPMI Manufacturer ID	0137h (311d) = IANA enterprise number for Microsoft 0157h (343d) = IANA enterprise number for Intel The value logged depends on the Intelligent Management Bus Driver (IMBDRV) that is loaded.
11	Record ID	Sequential number reflecting the order in which the records are read. The numbers start at one for the first entry in the SEL and continue sequentially to *n*, the number of entries in the SEL.
12–15	Shutdown Comment	Shutdown Comment from the registry (least significant bit first): HKLM/Software/Microsoft/Windows/CurrentVersion/Reliability/shutdown/Comment
16	Reserved	00h

14.3 Bug Check/Blue Screen Event Records

When the system experiences a bug check (blue screen), multiple records are written to the event log. The first record could be a Bug Check, Blue Screen OS Stop, or Shutdown Event Record followed by multiple Bug Check/Blue Screen code OEM records that contain the Bug Check/Blue Screen codes. This information can be used to determine what caused the failure.

Table 134. Bug Check/Blue Screen – operating system stop event record typical characteristics

Byte	Field	Description
8, 9	Generator ID	0041h – System Software with an ID = 20h
11	Sensor Type	20h = Operating system Stop/Shutdown
12	Sensor Number	00h
13	Event Direction and Event Type	[7] Event direction 0b = Assertion Event 1b = Deassertion Event [6:0] Event Type = 6Fh (Sensor Specific)
14	Event Data 1	[7:6] – 00b = Unspecified Event Data 2 [5:4] – 00b = Unspecified Event Data 3 [3:0] – Event Trigger Offset = 1h = Runtime Critical Stop (that is, “core dump”, “blue screen”)
15	Event Data 2	Not used
16	Event Data 3	Not used

Table 135. Bug Check/Blue Screen code OEM event record typical characteristics

Byte	Field	Description
1, 2	Record ID	ID used for SEL Record access
3	Record Type	[7:0] – DEh = OEM timestamped, bytes 8–16 OEM defined
4–7	Timestamp	Time when the event was logged. The least significant byte is first.
8–10	IPMI Manufacturer ID	0137h (311d) = IANA enterprise number for Microsoft 0157h (343d) = IANA enterprise number for Intel The value logged depends on the Intelligent Management Bus Driver (IMBDRV) that is loaded.
11	Sequence Number	Sequential number reflecting the order in which the records are read. The numbers start at 1 for the first entry in the SEL and continue sequentially to *n*, the number of entries in the SEL.
12–15	Bug Check/Blue Screen Data	The first record of this type contains the Bug Check/Blue Screen Stop code and is followed by the four Bug Check/Blue Screen parameters. The east significant byte is first. Each of the Bug Check/Blue Screen parameters requires two records each. Both of the two records for each parameter have the same Record ID. There is a total of nine records.
16	Operating system type	00 = 32-bit operating system 01 = 64-bit operating system

15. Linux* Kernel Panic Records

The OpenIPMI driver supports the ability to put semi-custom and custom events in the system event log if a panic occurs. Enable the “Generate a panic event to all BMCs on a panic” option to get one event on a panic in a standard IPMI event format. Enable the “Generate OEM events containing the panic string” option to get a set of OEM events holding the panic string.

Table 136. Linux* kernel panic event record characteristics

Byte	Field	Description
8, 9	Generator ID	0021h – Kernel
10	EvM Rev	03h = IPMI 1.0 format
11	Sensor Type	20h = Operating system Stop/Shutdown
12	Sensor Number	The first byte of the panic string (0 if no panic string)
13	Event Direction and Event Type	[7] Event direction 0b = Assertion Event 1b = Deassertion Event [6:0] Event Type = 6Fh (Sensor Specific)
14	Event Data 1	[7:6] – 10b = OEM code in Event Data 2 [5:4] – 10b = OEM code in Event Data 3 [3:0] – Event Trigger Offset = 1h = Runtime Critical Stop (a.k.a. “core dump”, “blue screen”)
15	Event Data 2	The second byte of the panic string
16	Event Data 3	The third byte of the panic string

Table 137. Linux* kernel panic string extended record characteristics

Byte	Field	Description
1, 2	Record ID	ID used for SEL Record access
3	Record Type	[7:0] – F0h = OEM non-timestamped, bytes 4–16 OEM defined
4	Secondary Address	The secondary address of the card saving the panic
5	Sequence Number	A sequence number (starting at zero)
6–16	Kernel Panic Data	These hold the panic sting. If the panic string is longer than 11 bytes, multiple messages are sent with increasing sequence numbers.

Appendix A. Glossary

Term	Definition
ACPI	Advanced Configuration and Power Interface
AER	Advanced Error Reporting
BIOS	Basic Input/Output System
BMC	Baseboard Management Controller
CATERR	Catastrophic Error
CFM	Cubic Feet per Minute
CLST	Closed Loop System Throttling
DIMM	Dual Inline Memory Module
DLLP	Data Link Layer Packet
DTS	Digital Thermal Sensor
ECC	Error Correction Code
EWS	Embedded Web Server
FP	Front Panel
FRU	Field Replaceable Unity
GPGPU	General-purpose computing on graphics processing unit
HDD	Hard Disk Drive
HSC	Hot-Swap Controller
HSBP	Hot-Swap Backplane
IANA	Internet Assigned Numbers Authority
IERR	Internal Error
IPMI	Intelligent Platform Management Interface
IPMB	Intelligent Platform Management Bus
LUN	Logical Unit Number
MCTP	Management Component Transport Protocol
Intel® ME	Intel® Management Engine
MSR	Model Specific Register
NIC	Network Interface Controller
Intel® NM	Intel® Node Manager
NMI	Non-Maskable Interrupt
OEM	Original Equipment Manufacturer
OOB	Out-of-band
OS	Operating System
PCH	Platform Controller Hub
PCIe*	PCI Express*
PECI	Platform Environmental Control Interface
PEF	Platform Event Filters
PERR	Parity Error
POST	Power On Self-Test
PSU	Power Supply Unit
PWM	Pulse Width Modulation
Intel® QPI	Intel® QuickPath Interconnect
RAS	Reliability, Availability, Serviceability
RqSA	Requester's Secondary Address

Term	Definition
SAS	Serial Attached SCSI
SATA	Serial ATA
SCMP	Software Configuration Management Plan
SDR	Sensor Data Record
SmaRT	Smart Ride Through
SEL	System Event Log
SERR	System Error
SMI	System Management Interrupt
SSB	South Side Bridge
TLP	Transaction Layer Packet
TPS	Technical Product Specification
TSOD	Temperature Sensor on DIMM
VR	Voltage Regulator
VSCC	Vendor Specific Component Capabilities